BME Design-Spring 2025 - Richard YANG Complete Notebook

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ELLIOTT HARRIS

on

May 04, 2025 @11:20 PM CDT

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Team contact Information

Ellie Dingel - May 04, 2025, 5:54 PM CDT

Last Name	First Name	Role	E-mail Phone Of		Office Room/Building
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Dingel	Ellie	Communicator	dingle@wisc.edu	608-797-8346	
Rice	Mark	BSAC	mjrice2@wisc.edu	715-252-2247	
Harris	Elliott	BWIG	epharris2@wisc.edu	414-336-4974	
Harris	Elliott	BPAG	epharris2@wisc.edu	414-336-4974	

Comments

Amit Nimunkar

Please add the Team contact information.

Apr 04, 2025, 10:14 AM CDT



Ellie Dingel - May 04, 2025, 2:52 PM CDT

Course Number: BME 402

Project Name: Diagnostic EEG for viral-induced epilepsy

Short Name: EEG for Epilepsy

Project description/problem statement:

Problem Statement:

Epilepsy is recognized as a potential consequence of infection by endemic viral pathogens prevalent in developing regions. Unfortunately, the diagnostic capability to localize seizure foci is severely restricted in low-resource medical environments where access to electroencephalography (EEG) is limited. Despite this well-documented risk, many medical facilities in low-resource settings lack the necessary diagnostic tools, such as EEG, to effectively localize seizure foci. The inability to pinpoint these foci impedes timely and precise treatment, exacerbating the burden of epilepsy in these communities. This project aims to address this critical gap by developing an affordable, open-source EEG system tailored for rapid deployment in rural and under-resourced hospitals. By enhancing the localization and treatment of epilepsy, this initiative seeks to significantly improve clinical outcomes in regions with limited healthcare infrastructure.

Project Description:

Epilepsy is a prevalent neurological disorder affecting approximately 50 million people worldwide, with 80% of cases occurring in low- and middleincome countries where access to diagnostic tools like electroencephalograms (EEGs) is limited. Conventional EEG devices are prohibitively expensive, restricting early diagnosis and treatment planning. This study presents the development of an affordable, portable, and reliable 10-channel EEG system for diagnosing viral-induced epilepsy, with a targeted production cost of under \$100. The system comprises a custom-designed printed circuit board (PCB) for signal acquisition and amplification, a 3D-printed head cap for electrode placement, and an embedded system for real-time signal processing and data transmission. The analog front-end utilizes a Raspberry Pi RP2040 microcontroller, an instrumentation amplifier, and a multiplexer-based architecture to enhance signal fidelity while minimizing switching artifacts. The system achieves an average CMRR of 65.1 dB and SNR of 24.5 dB and captures evoked biopential from blinking. A GUI can display all ten channel in realtime with configurable parameters. The embedded system timing achieves a standard deviation of 0.24 µs in sampling period. The electronics component (not including the PCB) cost \$42. Future work will focus on refining the head cap design for broader fitment, improving ear clip durability, and optimizing the analog circuitry for enhanced signal quality. This EEG system costs less than \$100 and has the potential to significantly improve epilepsy diagnostics in resource-limited settings, enabling earlier intervention and better patient outcomes.

About the client:

Dr. Coventry received a B.S. in Electrical Engineering from Saint Louis University and a M.S.E.C.E and PhD in Biomedical Engineering from Purdue University. He is interested in using optical tools and artificial intelligence in thalamocortical circuits to improve neuromodulation strategies for the clinic. He is currently a post doctoral fellow in the department of Neurological Surgery.

Dr. Brandon Coventry Neurological Surgery UW School of Medicine and Public Health COVENTRY@WiSC.edu (217) 853-1585

Comments

Amit Nimunkar

Please complete this entry.

Apr 04, 2025, 10:14 AM CDT



Ellie Dingel - May 04, 2025, 6:47 PM CDT

Title: Client Meeting 3.21

Date: 3.21.2025

Content by: Ellie Dingel

Present: Ellie / Richard

Goals: To print the pcb

Content:

- Needed to print the PCB that was created
- Compiled all necessary files, they are included in the fabrication section of notebook
- Allowed for feedback if needed, but said board looked good
- Ensured was printed so should get after returning from spring break

Conclusion:

Collect PCB after printing so can begin testing as soon as possible



Ellie Dingel - May 04, 2025, 6:21 PM CDT

Title: Advisor Meeting 2.14

Date: 2.14.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

Content:

- Tried to verify gain of analog front end
- Percent difference comes from the first stage
- More chance of error is the resistors, so can split up the amplifier if need to
- Moving forward will work on the driven right leg
- Head cap contains all the electrodes that are required
- This working prototype can be modeled and be used for testing purposes
- Have to work on creating a more universal design for the electrode cap

Action items:

- Get together and figure out head cap design (if need to change ideas, what that looks like, etc.)
- Continue to work and modify the ear clip
- Contact someone about why cap / gel / etc is utilized
- Potentially see some of the device
- Continue working on circuitry

Conclusion:

Use advice going forward to help project



Ellie Dingel - May 04, 2025, 6:22 PM CDT

Title: Advisor Meeting 2.21

Date: 2.21.2025

Content by: Ellie Dingel

Present: Team

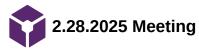
Goals: To present work that has been done surrounding the project

Content:

- Presented work on DRL
- Can test two circuits, one with DRL and one without
- Continue to work on circuit
- Get outreach done as soon as possible
- Can share code to get SPI in contact with the circuit
- Have to test circuit with the embedded system
- As a group have to decide how much work to put in cap
- Don't want two incomplete projects, so should at least finish earclip
- Want more clarification on the earclip
- Try to get the earclip done, can test it, then can put all energy into headcap
- Print the new earclip design, then test within us

Conclusion:

Use advice and follow plan going forward



Ellie Dingel - May 04, 2025, 6:22 PM CDT

Title: Advisor Meeting 2.28

Date: 2.28.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

Content:

- Rheostat can be powered with two power supplied
- Automatically set to 50k, got reading of 47k
- Can use logic analyzer to see if sending out command (1. code itself is wrong 2. sending command but not correct)
- Mux working on breadboard
- buy adaptors for safety pins (have header pins for testing, need safety pins)
- Work with the I2C
- Testing with the driven right leg circuit
- Ear clip is finished
- Headcap may not be needed, can just place the electrodes where they are needed
- Ellie: Talk with royal and see if can get force sensor
- Draft protocol for earclip testing

Action items for everyone

- Mark: continue embedded system
- Richard: work to draft protocol, help embedded system, connectors for testing, driven right leg testing
- Ellie: Talk royal and see if can get force sensor, help with drafting protocol, driven right leg testing
- Elliott: Work on testing for earclip, work on drafting protocol
- Have insert different thickness, use force sensor to test it

Conclusion:

Each work on action items.



Ellie Dingel - May 04, 2025, 6:29 PM CDT

Title: Advisor Meeting 3.7

Date: 3.7.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

Content:

- GUI has been complete
- Work on the rheostat, can add connectors for resistor values
- Can have issues with reading and writing if not careful
- Pico has a way to help prevent this
- Was able to acquire data from sampling and preform some analysis
- Testing was conducted on the earclip between the average size
- Got results that were less than the pressure ulcer
- Solidify the testing results for the earclip
- Able to figure out code with the rheo, think the issue comes from inadequate power

Conclusion:

Continueto work on circuit



Ellie Dingel - May 04, 2025, 6:29 PM CDT

Title: Advisor Meeting 3.7

Date: 3.14.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

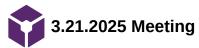
Content:

- can use amplitude modulation from the signal generator for testing
- previously calculated CMRR and SNR, but need to red calculations for CMRR
- For SNR want to do FFT of input signal (into circuit) and output signal of circuit
- Also fix units on y axis, don't have 700 V

- 3 different types noise (60hz noise that comes from environment - capacitively coupled in; second noise is the low frequency drift; 3rd noise is motion artifacts from electrodes moving on the skin)

Conclusion:

Redo calculations as necessary



Ellie Dingel - May 04, 2025, 6:31 PM CDT

Title: Advisor Meeting 3.7

Date: 3.21.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

Content:

- Mark worked on timing the interrupt to see if it was what was expected.

- Worked and saw that the timing between interrupts was about 100 microseconds, which is close to the sampling rate we should get.

- Team has finished the routing for the pcb
- Team is meeting with client to confirm design and print the circuit board following advisor meeting
- Board will hopefully arrive right after spring break

Conclusion:

Team should ensure board is printed before break



Ellie Dingel - May 04, 2025, 6:34 PM CDT

Title: Advisor Meeting 4.18

Date: 4.18.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

Content:

- Mark printed case for circuit board
- Mark and Elliott plan to do testing on durability of case
- Elliott emailed wiseman center, they have not responded to next email
- Want to investigate what does an EEG look like
- Will test with evoked potential to see how it can work
- What would client want to see out of project
- Acquire signal from the pcb

Conclusion:

Need to ensure that can acquire signal from pcb



Ellie Dingel - May 04, 2025, 6:37 PM CDT

Title: Advisor Meeting 5.2

Date: 5.2.2025

Content by: Ellie Dingel

Present: Team

Goals: To present work that has been done surrounding the project

Content:

-Team had poster presentation

- Everything went well
- Client was very happy with the output of the project
- Team should work on refining the final paper for submission
- Lots of comments were made on the final document, refer to there for specifics

- Client would like to submit this for publication - as such, should ensure has all the necessary components for submission. Also, this may affect some of the content that is included in the design.

Conclusion:

Team will work to finalize the journal article for submission



5.2.2025 PCB Component Expenses

Ellie Dingel - May 04, 2025, 6:42 PM CDT

Title: PCB Components Expenses

Date: 5.2.2025

Content by: Ellie Dingel

Present: N/A

Goals: To detail the circuit components cost

Content:

Following is a table with all the expenses of each circuit component

Component	Manufacturer	Manufacturer Part#	Cost Each	QTY	Total
Instrumentation Amplifier	Texas Instrument	INA827AIDGKR	1.906	10	19.06
Multiplexer	Texas Instrument	CD74HC4067M96	0.57	1	0.57
Microcontroller	Rasberry Pi	RP2040	4	1	4
Operational Amplifier	Texas Instrument	TLV9004IDR	0.408	8	3.264
Operational Amplifier	Texas Instrument	TL072CDR	0.26	1	0.26
Male Header	Samtec	HTSW-108-07-G-D	0.9	1	0.9
.1uF capacitor	Samsung Electro-Mechanics	CL10B104KA8NNNC	0.004	55	0.22
10uF capacitor	Samsung Electro-Mechanics	CAP CER 10UF 10V X5R 0603	0.032	9	0.288
100uF cappacitor	Samsung Electro-Mechanics	CL31A107MQHNNNE	0.52	1	0.52
220pF capacitor	Samsung Electro-Mechanics	CAP CER 220PF 50V X7R 0603	0.027	6	0.162
DC-DC convertor	ТС962ЕРА	TC962EPA-ND	4.09	1	4.09
10K Resistor	Stackpole Electronics Inc	RAVF164DJT10K0	0.022	2	0.044
20K Resistor	Stackpole Electronics Inc	RAVF164DJT20K0	0.03	2	0.06
390K Resistor	Stackpole Electronics Inc	RMCF0603FT390K	0.02	4	0.08
160K Resistor	Stackpole Electronics Inc	RMCF0603FT160K	0.02	6	0.12
470 Resistor	Stackpole Electronics Inc	RMCF0603JT470R	0.019	6	0.114
1K Resistor	Stackpole Electronics Inc	RMCF0603FT1K00	0.02	2	0.04
360 Resistor	Stackpole Electronics Inc	RMCF0603FT360R	0.02	8	0.16
180 Resistor	Stackpole Electronics Inc	RMCF0603JT180R	0.019	4	0.076
4.3M Resistor	Stackpole Electronics Inc	RMCF0603FT4M30	0.024	6	0.144
10K potentiometer	Same Sky (Formerly CUI Devices)	PT01-B120D-B103	0.758	10	7.58
				Total	41.752

Conclusion:

Use these components to populate the circuit board.



Ellie Dingel - May 04, 2025, 6:15 PM CDT

Title: PCB Files for Fabrication

Date: 5.4.24

Content by: Ellie Dingel

Present: NA

Goals: To have the files required to print the PCB of V2 for the board

Content:

Attached are all of the files required to print the pcb of our board. These files can be submitted to a printing service without any alterations. This allows for anyone to print the board.

Conclusion:

These files should be uploaded to a Github so that they can be accessed by anyone.

Ellie Dingel - May 04, 2025, 6:16 PM CDT



<u>Download</u>

pcb_files_printing.zip (151 kB)

11.20 CMRR Testing Protocol

Ellie Dingel - Nov 20, 2024, 7:47 PM CST

Title: CMRR Testing Protcol

Date: 11.20.24

Content by: Ellie Dingel

Present: NA

Goals: To create a testing protocol for the CMRR of the circuit

Content:

The testing is located below, and is also attached to these notes.

Stage 1 - Testing without Mux

- 1. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.
- 2. Hook up the input of the first instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes of the first instrumental amplifier.
- 3. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.
- 4. Apply a 20Hz 100 μ V sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 μ V sine wave to the wave generator that is attached to both the input and reference input.
- 5. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.
- 6. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.
- 7. Perform calculations using the equation CMRR(dB)=20log10(GdifferentialGcommon), where the Gdifferential is the value of the output at 20Hz, and Gcommon is the value of the output at 60Hz. Both the Gdifferential and Gcommon should be expressed in voltage.
- 8. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.
- 9. Repeat this protocol with 5Hz, 10Hz, 15Hz, 25Hz, and 30Hz all replacing the 20 Hz signal, keeping the signal amplitude at 100 μ V.

Stage 2 - Testing with Mux

- 10. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.
- 11. Hook up the input of the instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes. All of the inputs for the instrumental amplifier should receive the same signal, as should all of the reference nodes.
- 12. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.
- 13. Apply a 20Hz 100 μ V sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 μ V sine wave to the wave generator that is attached to both the input and reference input.
- 14. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.
- 15. Inspect the data and note anything of significance that could account from the addition of the mux. This can include spikes or lapses in data.
- 16. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.
- 17. Perform calculations using the equation CMRR(dB)=20log10(GdifferentialGcommon), where the Gdifferential is the value of the output at 20Hz, and Gcommon is the value of the output at 60Hz. Both

Team activities/Testing and Results/Protocols/11.20 CMRR Testing Protocol

the Gdifferential and Gcommon should be expressed in voltage.

18. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.

Repeat this protocol with 5Hz and then 30Hz replacing the 20 Hz signal, keeping the signal amplitude at 100 µV.

Conclusion:

This testing protocol should be implemented to test the circuit.

Ellie Dingel - Nov 20, 2024, 7:47 PM CST

- Stape 1 Tasking without Max 1. Place the circuit based on cloud, connecting all necessary components that are not permanently attached, separat the circuit based to ensure that a connections are sold and all components are placed connectly. 2. Hook up the input of the flat intriumental amplifier to a wave generated, and hook up a second wave generate for black the input and the income reade at the flat instrumental amplifier. 3. Set up these oscillators produce, and one to measure the input at the instrumental amp, one to measure the input at the reference prote, and one to measure the output of the onion.

- cited1
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- citoph. 13. Apply a 2015:100 μV sine wave to the input of the instrume risk amplifier. Apply a 60 Hz, 10 μV sine wave to the wave generator that is attached to both the input and softwares input.

Download

CMRR_Testing_Protocol.pdf (79.2 kB)



Richard YANG - Nov 21, 2024, 7:45 PM CST

Richard YANG - Nov 21, 2024, 7:45 PM CST

Title: PSRR protocol

Date: 11/21

Content by: Richard

Present: NA

Goals: sketch protocol outline

Content:

Materials:

- 1. AC+DC network summing device
- 2. Oscilloscope (ideally one that can automate frequency sweep)

 $PSRR = 20 \log (\Delta vin / \Delta vout)$

Protocol:

- 1. Connect 5V DC to the summing device and an AC source with 100mV PtP
- 2. Connect the recording electrode and reference to 1V DC
- 3. Observe the PtP ripple amplitude at Vout
- 4. calculate PSRR

Conclusions/action items:

Bode 100 device can also be helpful if avaliable



<u>Download</u>

PSRR_Measurement.pdf (217 kB)

4.17 Drop Testing Protocol

Ellie Dingel - May 04, 2025, 6:08 PM CDT

Title: Drop Testing Protocol

Date: 4/17/2025

Content by: Mark Rice

Present: Mark

Goals: Develop a protocol for testing the case for drop testing damage.

Content:

Objective:

evaluate the durability of the EEG cap case prototype from common wear and tear use like accidental drops.

Scope

This will be done with a empty circuit board since we do not have extra components that can be damaged, further work can be considered with a full circuit prototype on board to evaluate if it can still function. For now it will look for cosmetic damage, damage to the circuitboard and how well the board stays screwed in.

Test Equipment

Calipers, phone camera for video and photo analysis, 1 3d printed prototype made from PLA for damage testing and 1 for an undamaged control, hard floor like concrete, wood, stone etc.

Drop heights

0.75 m, 1m, 1.2m or as necessary to see damage

Drop orientations (starting in this position):

Flat on base

Flat on top

Flat on front face

Flat on back face

Flat on left side

Flat on right side

One top front edge

One corner

Test procedure:

starting at 0.75m, randomly select an orientation and drop while recording with a camera. Take photos of any changes in damage, record if the damage is: cosmetic, functional and if the damage is: minor (can still be used for normal function) moderate (still works but is badly cosmetically damaged) or severe (cannot continue under normal function).

Acceptance criteria

The product is acceptable if it makes it through all orientations at all 3 heights with only receiving minor or moderate cosmetic damage, not severe damage.

Conclusions/action items:

I plan to look over this protocol with the team tomorrow and conduct the testing with Elliot as well if it looks good.



Ellie Dingel - May 04, 2025, 6:52 PM CDT

Title: Circuit Problem Solving

Date: 2.12.25

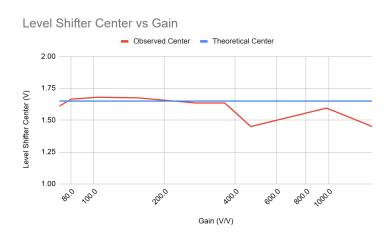
Content by: Ellie, Richard

Present: Richard, Ellie

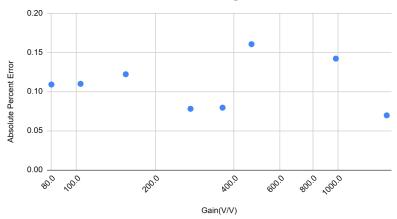
Goals: To verify the gain on the circuit

Content:

Circuit was taken to the makerspace and the gain was tested. Through the data, the following graphs were obtained. This helped to prove that the gain is within acceptable tolerances for the circuit, as stated in the PDS.

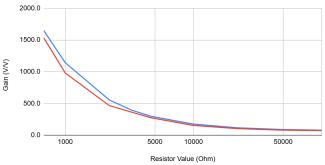


Theoritical Gain Overall and Percentage Gain Diff



Team activities/Testing and Results/Experimentation/2.12 Circuit Gain verification





Conclusion:

This gain is acceptable. This data should be put within our final report and shared with the team.



Richard YANG - Feb 14, 2025, 1:51 PM CST

Title: Testing the gain of the analog frontend

Date: 2/12

Content by: Richard

Present: Richard, Ellie

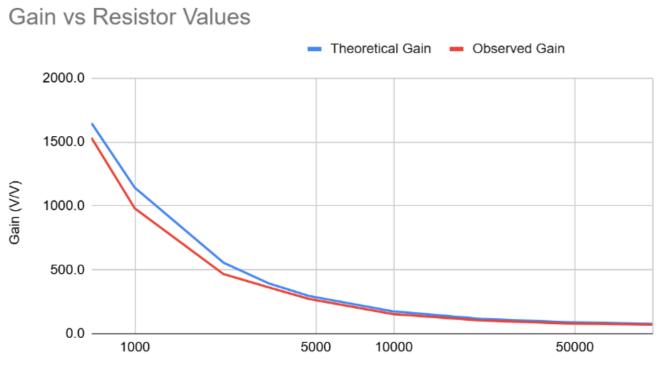
Goals: verify the gain of the analog frontend

Content:

https://docs.google.com/spreadsheets/d/1a-CB7LHxjFqJqh018v1t9h7aV8L39hX2GWohjg8Bads/edit?usp=sharing

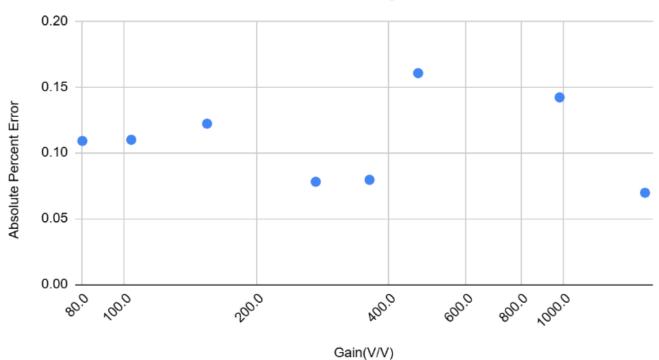
The chart below shows the comparison between the theoretical gain and the observed gain. The difference between them grow proportional to the magnitude of gain.

Overall this error is acceptable since we will still be able to properly amplify the signal. EEG signals generally have a range of 20uV to 300uV. With the lowest signal of 20uV, we will still be able to amplify it to 100mV. We also have a variable gain amplifier with a max gain of 210 V/V after this stage, so the signal is well situated in the optimal range.

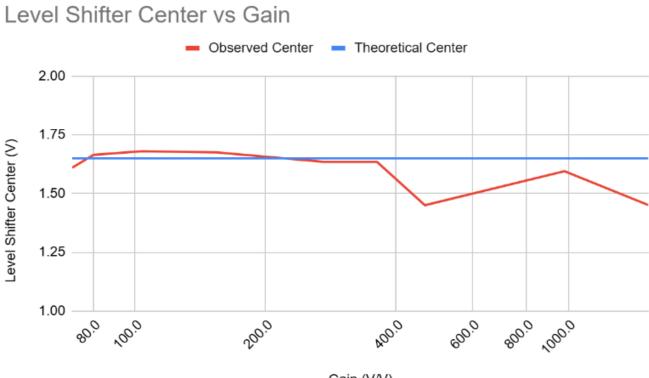


Resistor Value (Ohm)

The chart below shows the absolute percent error of the observed gain from the theoretical gain. The percent error is consistent with an average of 11% and a standard deviation of 3%.



The average of level shifter center is 1.6 V, corresponding to a 3% average error.



Gain (V/V)

Team activities/Testing and Results/Experimentation/2/12_circuitVerification

Debug the first channel and then the drl.



Richard YANG - Feb 15, 2025, 1:55 PM CST

Title: circuit verification

Date: 2/14

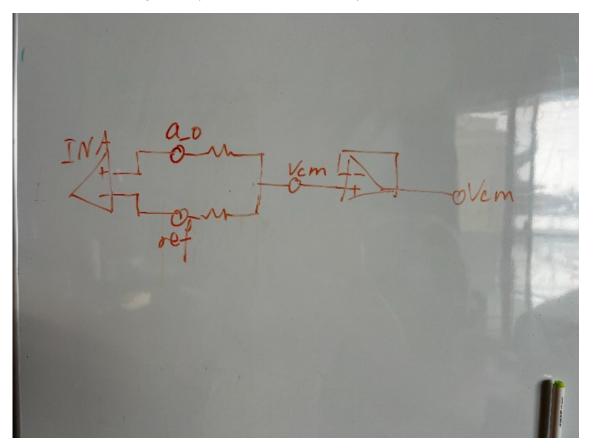
Content by: Richard

Present: Richard, Ellie

Goals: debug the driven right leg circuit

Content:

The driven right leg circuit amplifies and invert the input signal correctly; however, we failed to obtain the common mode signal. I believe this is due to employing the resistor network too late in the signal processing task where the common mode signal has largely been filtered out. To more effectively obtain the common mode signal, the inputs should be connected directly to a resistor network.



Conclusions/action items:

Experiment with this on breadboard.



Ellie Dingel - May 04, 2025, 6:51 PM CDT

Title: Testing of the Rheostat

Date: 2.26.25

Content by: Ellie

Present: Ellie, Mark, Richard

Goals: Figure out why the digital rheostat isn't working

Content:

We attempted to test the circuit, but were unsuccessful. We noted that the Vss and Vcc pins can be easily shorted and cause damage, which caused us to order more. I have put together a digikey order to accomplish this.

The rheostat, once turned on, gave a value of 50kOhms. However, we were not able to change this value. It was sent to 50Kohms no matter what. The code was rechecked, as was the communication, however the issue could not be located. Testing will resume another day to try and address the issue.

The rest of the circuit was tested using this 50kohm value, and it was proved to be successful.

Conclusion:

We will need to figure out the error that is causing issues. Once this is tackled, we can test how effective the MUX is and continue to V2 of the circuit.



Richard YANG - Mar 05, 2025, 3:41 PM CST

Title: embedded testing

Date: 3/5

Content by: Richard

Present: Richard, Ellie

Goals: test the MUX

Content:

we can reliably obtain signal from channel 1 and 3 in the parallel configuration (until the channel 3 rheostat went offline).

We see that channels 5-10 display the same signal as channel 1 despite not being connected to any singal or not populated.

Conclusions/action items:

debug the rheostat, consider replacing it with a resistor just to test the channel configurations



Ellie Dingel - Mar 07, 2025, 12:27 PM CST

Download

PXL_20250305_202112760.jpg (2.15 MB)



Ellie Dingel - May 04, 2025, 6:51 PM CDT

Title: CMRR and SNR Testing

Date: 3.13.25

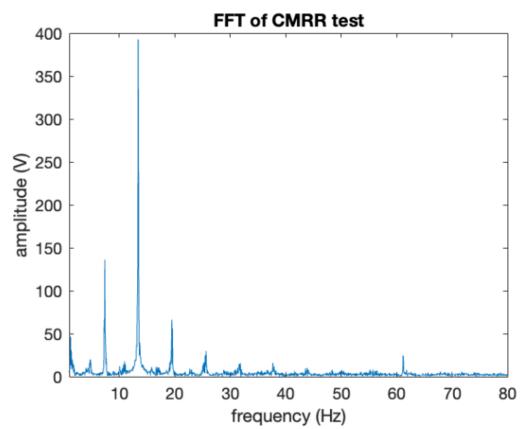
Content by: Ellie, Richard

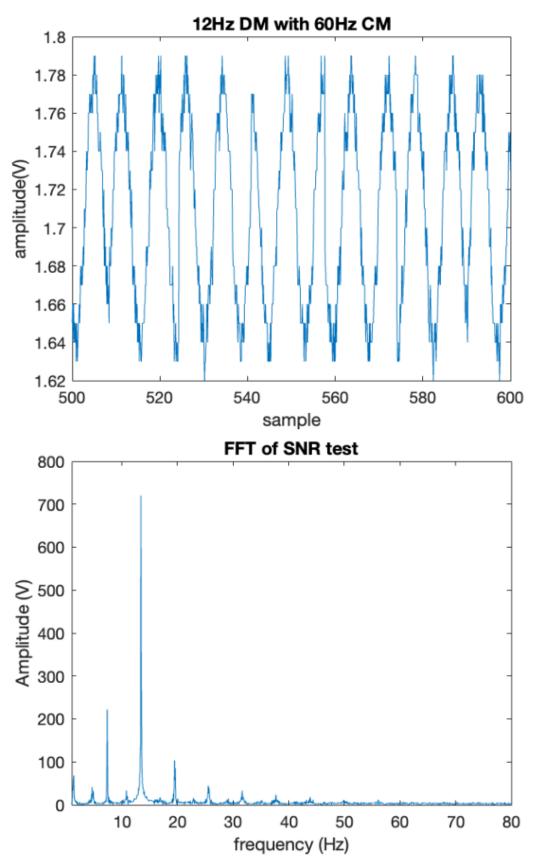
Present: Ellie, Richard

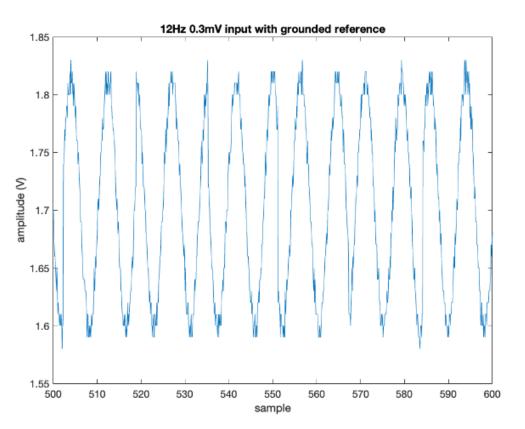
Goals: Provide more insight into CMRR and SNR

Content:

CMRR was conducted with a 120 mV signal at 12 Hz and a 20mV signal at 60 Hz. The CMRR was 2.65V/V, which is 8.5dB. For the SNR, there was a .3mV signal at 12 Hz untilized, which was tested against ground. The SNR was 3740V/V, which is 71.5dB. The graphs generated below by richard demonstrate the results that we achieved. These results are adequate given the scope of the project, and we will be utilized the configuration tested (parallel).







conclusion:

As this has given adequate results, we intent to begin crafting V2 of the circuit board. These results are deemed appropriate for our usage.



Richard YANG - Apr 04, 2025, 11:42 AM CDT

Title: review abnormal CMRR data

Date: 3/24

Content by: Richard

Present: Brandon

Goals: Discuss potential causes of abnormally low CMRR

Content:

1. Compared our architecture with existing architectures provided by the client. The only difference is the addition of active bandpass filter.

2. A potential source of error is the use of bread board, which might be noisy and add to the common mode gain

Updated testing method:

trial 1: CM gain

V-: 20mVsin(2pi60)

V+: 20mVsin(2pi60)

trial 2: DM gain

V-: 0

V+: 20mVsin(2pi12)

By separating the two trials, we can obtain cleaner data

Conclusions/action items:

Redo the CMRR test without the use of bread board



Richard YANG - Apr 04, 2025, 10:53 AM CDT

Title: ECG signal acquisition

Date: 3/24

Content by: Richard

Present: NA

Goals: Acquire a ECG signal as a sanity check

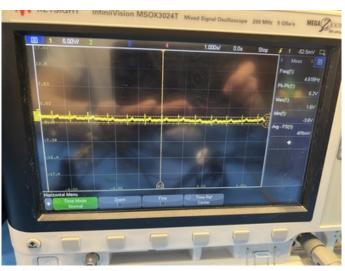
Content:

ECG signal can be acquired with the parallel configuration of the frontend. Previous attempts were unsuccessful due to excessive voltage gain in the instrumentation amplifier.

Conclusions/action items:

1. Assemble v2 when it arrives

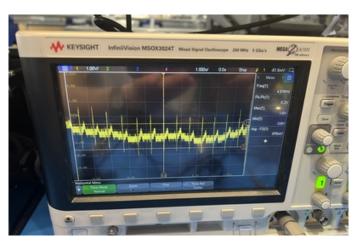
2. test driven right leg circuit



Richard YANG - Apr 04, 2025, 10:54 AM CDT

Download

IMG_7312_2.jpeg (2.63 MB)



Richard YANG - Apr 04, 2025, 10:54 AM CDT



<u>Download</u>

IMG_7313.jpeg (2.44 MB)



Ellie Dingel - May 04, 2025, 6:52 PM CDT

Title: EKG Acquisition

Date: 4.10.25

Content by: Ellie

Present: Ellie, Richard

Goals: To acquire EKG

Content:

We sat down to acquire EKG on GUI in order to have data. Ran into problems initially as the gain was not high enough. After switching out resistor, had correct gain but lots of noise issues. Decided to switch subjects from Ellie to Richard, which seemed to improve the quality. We were able to acquire a signal within the GUI, so should be able to process that data to provide visualization. This can help give us some data to compare to when we get the second version working. Below is an image of the data on the oscilloscope.



Conclusion:

Analyze the data in order to have a comparison metric for version two of the circuitry.



Ellie Dingel - May 04, 2025, 6:53 PM CDT

Title: Final Testing

Date: 4.21.2025

Content by: Ellie

Present: Ellie, Richard

Goals: Conclude testing on the circuit design

Content:

We were able to conduct lots of testing within this session. This testing includes:

1. Testing the evoked potential. We placed electrodes on the center of the forehead (in accordance with the 10-20 system), and then placed ground on the right mastoid and reference on the left mastoid. We were able to observe a signal which occurred both through blinking, as well as moving the eyes from left to right.

2. The driven right leg was tested. We were able to accomplish this by hooking up channel 1, both with the driven right leg connected and disconnected. The soldering iron was brought close to the circuit to cause interference. From observation, there was no difference. This will be analyzed further to see if there was any difference following the processing of the data.

3. The channels were fully populated, which helped to increase the accuracy and decrease the noise of the circuit.

4. Recording that occurred from all 10 channels at the same time. This helped to ensure that the mux was functioning properly and gave us confidence in our design.

Conclusion:

The results gathered from this testing data should be further processed and analyzed to draw conclusions from, as well as place on our final poster.



Ellie Dingel - May 04, 2025, 7:06 PM CDT

Title: Data Analysis for CMRR

Date: 4.22.2025

Content by: Ellie

Present: Ellie

Goals: Analyze the Data that was acquired during testing.

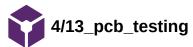
Content:

Got the results from testing both channel 1 and 2 at three different frequencies. These three frequencies should be analyzed to determine the CMRR for each of these. Coded in matlab to display the graphs for both the CM and the DM throughout the data. Using an FFT, also was able to acquire the CMRR for each of these three frequencies for the two different channels. The calculated values and the graphs are inserted below.

CH2 . 34AR 64 39aB 68.11aB 65.86 dB 1042 64.43dB 65.51dB

Conclusion:

Should be placed on the poster to present the data.



Richard YANG - Apr 17, 2025, 7:21 PM CDT

Title: pcb testing

Date: 4/13

Content by: Richard

Present: Ellie

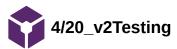
Goals: solder all components for channel 1

Content:

All components for channel 1 are soldered. Analog front ends for channels 2-4 are soldered as well.

Conclusions/action items:

Try to acquire a test signal and test the driven right leg circuit



Richard YANG - Apr 20, 2025, 6:05 PM CDT

Title: v2 testing

Date: 4/20

Content by: Richard

Present: NA

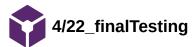
Goals: continue v2 testing

Content:

Conducted CMRR testing for channels 1 and 2. ECGs are also acquired from the two channels. Channel one requires significantly more gain to amplify the signal due to being tethered to the DRL circuit.

Conclusions/action items:

Analyze the data, calculate the CMRR/SNR, an continue testing



Richard YANG - Apr 23, 2025, 4:52 PM CDT

Title: final testing

Date: 4/22

Content by: Richard

Present: Ellie

Goals: conduct all testing

Content:

1. evoked potential. one electrode is attached between fp1 and fp2 according to the 10-20 system. reference electrode is attached to the left mastoid and the ground to the right mastoid. Evoked potential is observed when blinking eyes or moving eyes left and right.

2. Driven right leg test with soldering iron. Channel 1 input is connected to a 10Hz signal generator and reference to ground. A soldering iron is brought close to the signal source.

two sets of data are collected: with driven right leg connected to ground, and driven right leg disconnected. There is no visually observable difference.

3. Fully populate the channels. After populating, the signal quality improved significantly. This might be attributed to eliminating floating end points.

4. Simultaneous recording of 10 channels. Two signal generators are used to alternate the signal source of each channel. For example, channel 1 to signal 1, chanel 2 to signal 2, channel 3 to signal 1, etc. Signal 1 is a 10 Hz 20mV sinusoid and signal 2 is a 1 Hz 20mV sinusoid. Since the channel swithing happend in order, we can be sure that MUX works correctly by alternating signal source.

Conclusions/action items:

analyze the data



Richard YANG - Apr 23, 2025, 4:53 PM CDT

<u>Download</u>

Screenshot_2025-04-22_at_4.57.04_PM.png (939 kB)



Richard YANG - Apr 23, 2025, 5:03 PM CDT

Title: data analysis

Date: 4/23

Content by: Richard

Present: NA

Goals: analyze the data in preparation for the poster presentation

Content:

1. SNR is calculated. The time domain signal is first transformed into the frequency domain using a modified Welch's method that zero-means each segment with 4096-point FFT and 1024-point overlap. This is done for channel 1 and 2, each at three different frequencies: 1, 10, and 100 Hz. P_signal is estimated to the area under the curve centered at f0 plus or minus 5 Hz. P_noise is the total area under the curve minus P_signal.

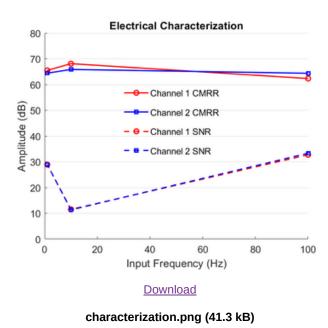
2. SNR is observed to dip at 10Hz. However, no significant changes in CMRR is observed. Thus, we can conclude that the signal strength is not affected in a frequency dependent manner, but the noise strength is. This could be due to insufficient conditioning of the power supply. '

3. Driven right leg testing result is analyzed. The spectral analysis is conducted the same way as SNR using a modified Welch's method. The SNR of the two test scenarios differs by around 1dB. Since we only have one sample is each category, no statistical test can be conducted.

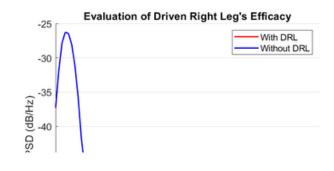
Conclusions/action items:

Prepare the poster presentation

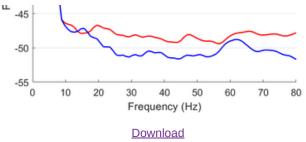
Richard YANG - Apr 23, 2025, 5:03 PM CDT



Richard YANG - Apr 23, 2025, 5:03 PM CDT

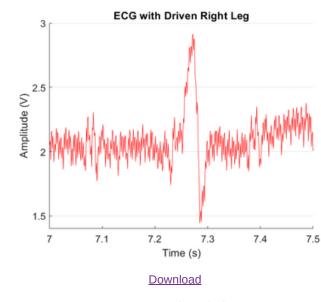


Team activities/Testing and Results/Experimentation/4/23_dataAnalysis



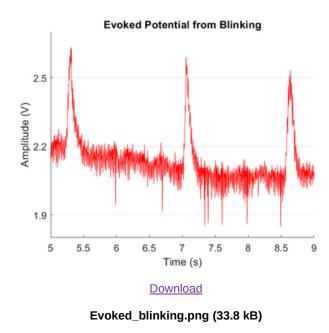
DRL.png (37.8 kB)

Richard YANG - Apr 23, 2025, 5:03 PM CDT



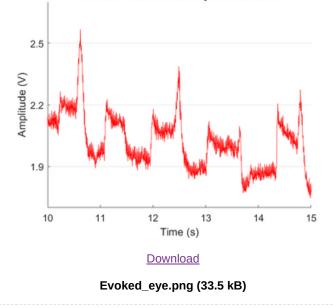
ECG.png (34.5 kB)

Richard YANG - Apr 23, 2025, 5:03 PM CDT

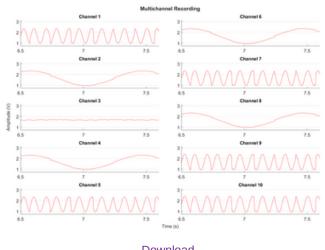


Richard YANG - Apr 23, 2025, 5:03 PM CDT

Evoked Potential from Eye Movements



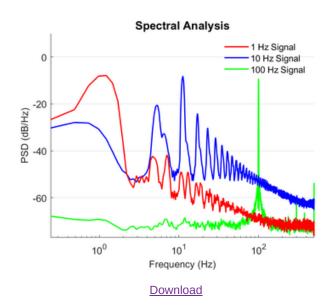
Richard YANG - Apr 23, 2025, 5:03 PM CDT



<u>Download</u>

multichannel.png (102 kB)

Richard YANG - Apr 23, 2025, 5:03 PM CDT





Ellie Dingel - Dec 11, 2024, 10:04 PM CST

Title: Design Matrix

Date: 12/11/24

Content by: Ellie / Full Team

Present: Full Team

Goals: To create a design matrix to analyze the designs that are presented

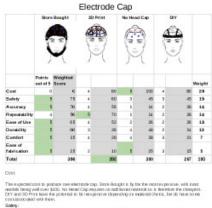
Content:

The document which includes the design matrix is attached. This document helped us to select the final design for both the headcap as well as the circuitry.

Conclusion:

The design matrix was created in order to analyze different designs presented by the team. This matrix helped to select the final design that was chosen.

Ellie Dingel - Dec 11, 2024, 10:09 PM CST

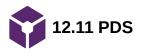


All electede cape should be talle for use and pervice trable electronic convectors, while noise of those design provide major m3, Silon Boxgir was matricale since it provides the instrupedectore between the electronice and lead while other disciple way to an type risk for electronics to come bose.

The observate cap design must help each electrotic accuracy at the associated body cal market. Since bragit may make the ensurement one with more material covering the least, statistic name electrotic citits in accurate to action at invitated by more material. Note: cap in the least

Download

Design_Matrix.docx (490 kB)



Ellie Dingel - Dec 11, 2024, 10:05 PM CST

Title: PDS
Date: 12/11/24
Content by: Ellie / Full Team
Present: Full Team
Goals: Create product specifications to ensure a design that meets the requirements.
Content:
The document which includes the pds attached. This document outlined the requirements that we had to meet while
designing the device. This will ensure that we meet client specifications.
Conclusion:
The pds will help to guide the team as the design is created; the team will reference this document often.
Ellie Dingel - Dec 11, 2024, 10:06 PM CST
Base A

Affordable Diagnostic EEG System for Viral-induced Epilepsy

Team Lead:	Richard Yang
Communicator:	Ellie Dingel
BSAC:	Mark Rice
EWIG & BPAC	Elliott Harris

Client Dr. Brandon Country Advisor: Professor Amit Nimunkar

Download

PDS.docx (192 kB)



Ellie Dingel - May 04, 2025, 6:03 PM CDT

Title: Preliminary Presentation

Date: 5/4/25

Content by: Ellie / Full Team

Present: Full Team

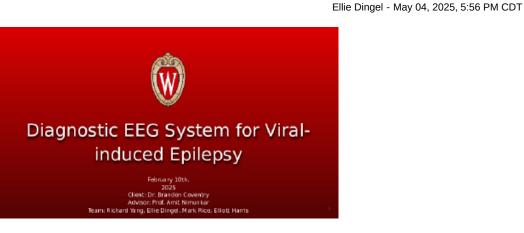
Goals: To give a preliminary presentation on our design

Content:

The document which includes the preliminary design presentation is attached. This document are the slides that were used to present our preliminary design to fellow design students.

Conclusion:

This project details what has been done with the project up to this point; this slideshow also includes future work and a direction to pursue for the remainder of the semester.



Download

preliminaryPresentation_Spring2025.pptx (5.32 MB)



Ellie Dingel - May 04, 2025, 6:02 PM CDT

Title: Preliminary Report

Date: 5/4/24

Content by: Ellie / Full Team

Present: Full Team

Goals: To create a preliminary report to present our design

Content:

The document which includes the preliminary report is attached. It is in the format of a journal article, similar to how the final report will be.

Conclusion:

This report details what has been done with the project thus far; the discussion and future work will be examined as the project continues.

Ellie Dingel - May 04, 2025, 5:57 PM CDT

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Download

Spring_25_prelimReport.docx (13.1 MB)



Ellie Dingel - May 04, 2025, 6:01 PM CDT

Title: Final Poster Presentation

Date: 5/4/24

Content by: Ellie / Full Team

Present: Full Team

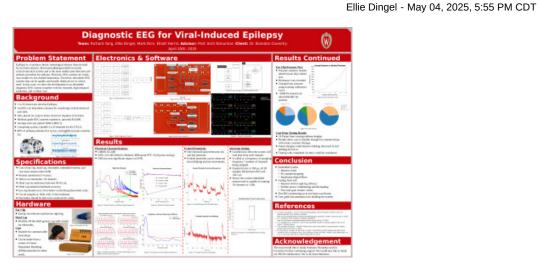
Goals: To document the final poster that was presented to fellow students.

Content:

The document which includes the final poster is attached. This document gives an overview of everything that has been accomplished this semester.

Conclusion:

This final poster details what the team has worked on over the course of the semester. This allows the team to present their findings to a larger audience.



Download

Spring2025_finalPoster.pptx (7.57 MB)



Ellie Dingel - May 04, 2025, 6:00 PM CDT

Title: Final Report

Date: 5/4/25

Content by: Ellie / Full Team

Present: Full Team

Goals: To document the final report for our design

Content:

The document which includes the final report is attached. This document is a journal article that outlines the project, including testing results, fabrication, and a discussion section.

Conclusion:

This report details what has been done with the project; this allows for extensive communication about everything that has occurred over the course of the semester.

Ellie Dingel - May 04, 2025, 5:57 PM CDT

Affordable Diagnostic EEG System for Viral-induced Epilepsy

Riched Yang¹¹, Ellic Dingef, Mark Rinn, Y. Ellin Horn, Annz Niemokari, and Banche Goverap¹⁰ Department el Risonched Explorating, University of Viscania-Madrine, Madrine M 13 NH USA Department el Sanger, University el Viscania-Madrine, Madrine M 15 NH USA Department el Sanger, University el Miscarcha-Madrine, Madrine M 15 NH USA Department el Sanger, University el Miscarcha-Madrine, Madrine M 15 NH USA Department el Sanger, University el Miscarcha-Madrine, Madrine M 15 NH USA Department el Sanger, University el Miscarcha-Madrine, Madrine M 15 NH USA "Conseptenting autor: Ramba Concept, con en grigh/siz.edu

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LINTRODUCTION

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Download

Spring_25_finalReport.docx (8.69 MB)



2024/12/10 Outreach brainstorming

Mark RICE - Dec 10, 2024, 1:36 PM CST

Title: Outreach Brainstorming

Date: 12/10/2024

Content by: Mark Rice

Present: Mark, will talk with team about this later as well.

Goals: brainstorm ideas for outreach plan for next semester.

Content:

Location:

- PODS (6-12th grade): in stevens point so may be out of most people's way and has not returned my messages to them.
- Lincoln Elementary (k-12 | think): I have done a program with them before, would have to be in the middle of the day on weekdays, last year I did 11-11:30 on Fridays for 6 weeks.
- Teens Like Us Support Group: LGBTQ support group for youth ages 13-18, has guest speakers sometimes. Could be fun to have a bit
 more mature of a conversation.

Activities:

- Saliva hormone test: would be hard and not sure if any of this is open source enough for us to easily do.
- EEG game & explanation: relates to our project and can tie in BME ideas into it. Can also just be a fun game to play.
- more LGBTQ focused could just be an overview of being queer in engineering and how queer issues relate to BME.

Conclusions/action items:

Will follow up on these during team meeting tonight

Mark RICE - Dec 10, 2024, 8:19 PM CST

- · sticks to make prosthetic hand
- water balloon throw (similar to initial thing



Ellie Dingel - May 04, 2025, 7:01 PM CDT

Title: Outreach Presentation

Date: 4.15.2025

Content by: Ellie, Team

Present: Team

Goals: Gather information to present to students about our activity

Content:

Attached is the presentation that we used for outreach .

Conclusion:

We will write up a reflection for our event

Ellie Dingel - May 04, 2025, 6:56 PM CDT



<u>Download</u>

Yang_Dingel_Harris_Rice_Outreach_Presentation.pptx (9.42 MB)



Ellie Dingel - May 04, 2025, 7:00 PM CDT

Title: Outreach Activity Guide

Date: 4.15.2025

Content by: Ellie, Team

Present: Team

Goals: Outline our plan for outreach activity

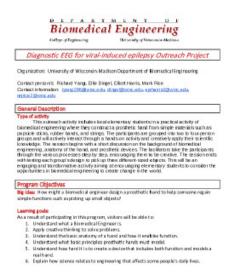
Content:

Attached is the activity guide that we used for outreach . This was presented to a class of 24 4th grade students at Randall Elementary.

Conclusion:

We will write up a reflection for our event

Ellie Dingel - May 04, 2025, 6:57 PM CDT



Download

Yang_Dingel_Harris_Rice_Outreach_ActivityGuide.docx (25.3 kB)



Ellie Dingel - May 04, 2025, 7:00 PM CDT

Title: Outreach Evaluation

Date: 4.15.2025

Content by: Ellie, Team

Present: Team

Goals: Evaluate our outreach presentation

Content:

Attached is the evaluation that was received from outreach.

Conclusion:

We will write up a reflection for our event

Ellie Dingel - May 04, 2025, 6:58 PM CDT

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Yang_Dingel_Harris_Rice_Outreach_Evaluation_1_.pdf (885 kB)



Ellie Dingel - May 04, 2025, 6:59 PM CDT

Title: Outreach Evaluation

Date: 4.16.2025

Content by: Ellie, Team

Present: Team

Goals: To summarize our outreach experience.

Content:

Attached is the reflection from our outreach experience.

Conclusion:

See if there are any future outreach activities can be involved in.



Ellie Dingel - Jan 24, 2025, 1:09 PM CST

Title: Team Meeting 1/24

Date: 1/24/2024

Content by: Ellie Dingel

Present: Team

Goals: Meet with team to discuss goals for the semester

Content:

Notes

- · Ideally at end of project test against industry standard
- · More focus on embedded system potentially as opposed to headcap
 - Mark might do more software
 - Elliot 3D design
 - Richard and Ellie hardware
- Mark has pi 5 available for testing
 - Needs to control multiplexer, rheostate (gain), and ADC
 - Needs to be delay in order to saturate bandpass filter for circuit where multiplexer comes before bandpass filter
 - Need to figure out sampling and switching in order to stabilize signal
- · Ellie send mark datasheets for the rheo, multiplexer, ADC
- Use a logic analyzer in order to see if circuit is functioning appropriately
- Increase header pins for next circuit board iteration

Timeline

- Jan 31st, sort out hardware channel
 - Richard and Ellie
- Feb 7th, pseudo-code for embedded
 - Mark
- End of Feb, full embedded done, start GUI
 - Mark
- March 21, v2 board
 - Richard and Ellie
- March 31st, start final testing
 - Richard and Ellie
- April 7th, start writing
 - Everyone

Outreach

- Date
- Supply
 - popsicle sticks
 - rubber bands
 - straws
 - Tape
 - Play dough
 - toothpicks
- Testing
- Email Organization

Team activities/Team Meetings/1.24 Team Meeting Notes

• Ellie do this

Upcoming Deadlines

- Select a suitable journal, Jan 31st
- Prelim Presentation, Feb 7th
- Prelim Deliverable, Feb 26th
- Executive summary and awards, Apr 4th
- Presentation, Apr 25th
- Final deliverable, Apr 30th

TODOs

- Semester goal
 - Functional system compared with industry standard in vivo (human)?
- Electrical
- Headcap
 - Might have to trim efforts on this to prioritize embedded?
- Embedded
- Meeting with Brandon?
- Timeline
- Outreach

Conclusion: The team should strive to achieve all of the goals set at each deadline. This will help to ensure that the project runs smoothly and is completed on time.



ELLIOTT HARRIS - Sep 20, 2024, 12:42 PM CDT

- Sep 23rd
 - Put together rough system designs for the design matrix
 - Friday Sep 27th Design Matrix due
- Sep 30th
 - Fully explore the chosen design
- Oct 7th
 - Wednesday Oct 9th Preliminary deliverables due
- Oct 14th
 - Finalize single-channel design
 - Begin bread-boarding/PCB fab
- Oct 21st
- Oct 28th
 - Friday Nov 1st Show and tell
- Nov 4th
 - Begin testing and validation
- Nov 11th
- Nov 18th
- Nov 25th
- Dec 2nd
 - Friday Dec 6th Presentation PDF due
- Dec 9th
 - Friday Dec 11th Final deliverables due

Comments

Amit Nimunkar

Please upload PDS for your project.

Sep 29, 2024, 9:36 AM CDT

2024/09/10 Physiological EEG & Viral induced epilepsy

Mark RICE - Sep 10, 2024, 3:48 PM CDT

Title: Physiological EEG & Viral induced epilepsy

Date: 9/10/2024

Content by: Mark Rice

Present: Mark

Goals: Understand physiological markers that are picked up by EEG, and what markers are given off by epilepsy and/or viral induced epilepsy

Content:

Virus-Induced Epilepsy vs. Epilepsy Patients Acquiring Viral Infection: Unravelling the Complex Relationship for Precision Treatment

- "Certain viruses can induce epilepsy by infecting the brain, leading to inflammation, damage, or abnormal electrical activity. Conversely, epilepsy patients may be more susceptible to viral infections due to factors, such as compromised immune systems, anticonvulsant drugs, or surgical interventions."
- "Unfortunately, the majority of the disease burden is borne by the developing world [45], which results in limited resources being allocated to deciphering how cestode brain infection ultimately triggers epilepsy as asserted by Steyn [46]."
- "During epilepsy, large numbers of neurons fire sequentially, resulting in non-synchronous electrical activity within the brain."
- "The basic mechanisms of focal seizure initiation and propagation include high-frequency bursts of action potentials, the hypersynchronization of a neuronal population resulting in spike discharge on an EEG."
- "Repetitive discharges lead to increased extracellular K+, accumulation of Ca2+ in presynaptic terminals, and NMDA receptor activation [129]."

Conclusions/action items:

Continue to read this.

2024/09/07- Raspberry Pi Research and Questions

Mark RICE - Sep 08, 2024, 3:04 PM CDT

Title: Raspberry Pi Research and Questions

Date: 9/7/2024

Content by: Mark Rice

Present: Mark

Goals: Understand what a raspberry pi is and is not capable of, and come up with questions for the client that may relate to this.

Content:

Differences between models:

- #of cores range between 1-4.
- CPU Clock speed: between 150 Mhz to 2.4 GHz
- Ethernet: likely not relevant to us.
- USB: likely not relevant to us but may effect peripherals later down the line
- Price: 5-75\$
- · GPU: depending on how we want to output results this may be a factor
- RAM: depending on the intensity of calculations this may be a factor to consider. 264 kb to 8 GB
- SPI
- I2C
- Wi-Fi / Bluetooth: may be helpful in case the PI cannot handle the calculations we can get a cheap pi and use Bluetooth to put the load of calculation on a phone or laptop instead, in this case the pi would only need to handle data collection and storage. (In this case built in memory like: SD, PCIe or built in storage may be relevant)

Raspberry pi is natively compatible with Python, C/C++ and Java, others may be possible to use if needed. Could use an ADC like this that will give 4 analog inputs per I2C port. Or something like this that would give 10 analog inputs to the raspberry Pi.

How do EEG collect data and output

- How do process and classify EEG signals. There is an open source Army Research Laboratory project that may be relevant. Written in python.
- "The (Arduino) Uno has 6 analog inputs, so you can observe 6 channels at once without any extra circuitry. If you want to observe more, you need a multiplexer chip such as the MAX4051. This chip will take as input a number of EEG channels and a number from 0-7, and output only the channel corresponding to the number. Rapidly cycling through the channels samples all of them at a rate necessary for good data acquisition."

What is EEG?

- "With certain exceptions, practically all patients with epilepsy will demonstrate characteristic EEG alterations during an epileptic seizure"
- "Most epilepsy patients also show characteristic interictal (or between-seizure) epileptiform discharges (IEDs) termed spike (<70 µsec duration), spike and wave, or sharp-wave (70–200 µsec duration) discharges."
- "The EEG is thought to be primarily generated by cortical pyramidal neurons in the cerebral cortex that are oriented perpendicularly to the brain's surface"
- "Temporary detachments of the recording electrodes (called "electrode pop" artifact) can further erode the EEG, or even imitate brain rhythms and seizures."
- "Digital filters may also be applied to reduce artifact in certain settings but must be used with great caution since they also filter EEG activity of interest and may distort EEG waveforms severely."
- "EEG uses the principle of differential amplification, or recording voltage differences between different points using a pair of electrodes that compares one active exploring electrode site with another neighboring or distant reference electrode."
- "The commonly used sensitivity is 7 μV/mm but can be adjusted up or down to make the EEG easier to visualize"
- We care about frequencies 1-30Hz, may want to notch filter at 60Hz

What is MEG and is it applicable to this project?

 "MEG, which does not record electrical activity but, rather, utilizes sensors to capture magnetic fields generated by the brain" -From What is EEG section

Questions for client:

Mark Rice/Research Notes/Biology and Physiology/2024/09/07- Raspberry Pi Research and Questions

2. What is the expected intensity that these calculations may be? Will we be needing one of the more powerful models or need to consider offloading calculation onto another computer.

Questions for further research:

What is SPI

What is I2C

What is a multiplexer chip

Conclusions/action items:

Have first meeting with client and ask about what Arduino we want to use, and number of channels etc.



Mark RICE - Oct 08, 2024, 4:34 PM CDT

Title: Open Source EEG Projects

Date: 9/18/2024

Content by: Mark Rice

Present: Mark

Goals:

- · Look at some open source EEG hardware systems
- · Look into electrodes and existing hardware

Content:

OpenBCI

- Open BCI Board based on Texas instrument ADS1299 could indeed be an effective alternative to traditional EEG Amplifiers
- 8 Channel board for 999\$ or 4 channel board for 499\$

FreeEEG32

- 32 channels for \$199 (entire board)
- uses STM32H743VGT6 which have 3x ADCs with 16 bit max resolution up to 36 channels up to 3.6 MSPS ~\$15
 - not sure what this is doing compared to the entire board aside from having spots to plug in electrodes and looks like an op amp and usb output?

ModularEEG

- 6* channels for 200-400\$
- Individual boards for ~80\$
 - · I am still not sure the differences in price for these boards and what they are doing

Ongoing? project VolksEEG

• unclear if this project is still ongoing or if a final prototype was completed.

Conclusions/action items:

Continue looking into what is needed for other hardware costs to start to break down what we may need.

I am having issues understanding what I am looking at or for in a lot of this, I could use some help understanding or maybe passing this on to someone with more of an electronics background.

Mark RICE - Oct 08, 2024, 4:35 PM CDT

Date: 9/19-20/2024

Content:

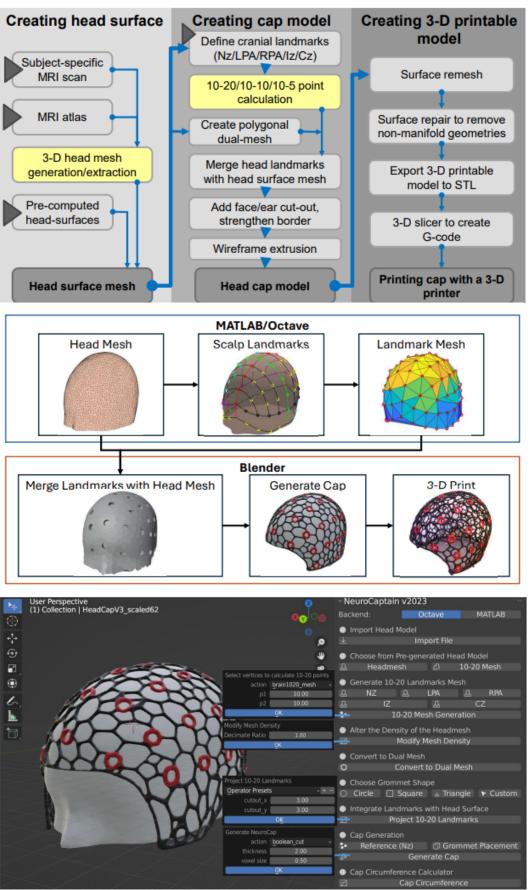
electrodes:

<u>10 for ~\$9</u>

10 for ~\$8

New electrode caps seem quite expensive, used or cheaper ones can be found for about 15\$.

Could <u>print</u> one in TPU, this would be adjustable for each size and wouldn't need a "one size fits all". Based on <u>this</u> paper. ~21g of filament, assuming no supports are used. Cost of TPU ranges from \$0.3-0.8 per gram, so estimated cost of material = \$6.3 - 16.80. Paper used supports causing a lot more material for cost of cap to be \$31.36.



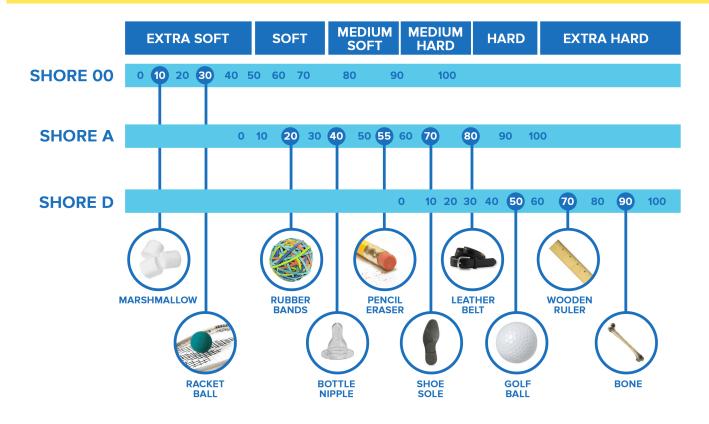
Paper wants to use a patient specific MRI scan to get 3-D head mesh, not sure if this is necessary. I wonder if we could use like a mobile phone app to get an okay approximation or just have a few that are general fitting sizes like S-M-L. Could play around with blender settings to optimize the strength and minimize amount of material or look into printing with other flexible 3d printable materials.

^This would be an interesting part of the project for me to dive further into, maybe optimizing this for lower cost. I also would like to learn blender and this would be a good opportunity for that.

Do the metal types effect quality? If so, is better quality worth it since we want this to be as cheap as possible?

Name (Flexible filament)	Cost/gram	Flexibility (Shore Hardness) Lower is more flexible	Printing Temp (deg C)
TPU	0.3-0.8	60A-77D	210-230
Soft PLA	0.12	92A	190-230
TPA / TPI	0.39	70A-95A	230-250
РЕВА	0.16	75A-90A	240-260
TPC	0.052	95A	220-260
TPS	0.08	70A-90A	260-280

Shore Hardness Scale



Date: 10/16/2024

Met with makerspace regarding this, will have follow-up appointments to get this printed.

Also: following up with Dr. Fang regarding the blender plugin to get that working.

Mark RICE - Feb 04, 2025, 2:08 PM CST

Title: GUI Brainstorming

Date: 2/4/2025

Content by: Mark Rice

Present: Mark

Goals: Brainstorm how to go about GUI for this project

Content:

This video goes over how to read data from a USB device, PyUSB library may be a good place to start looking. Still wondering about how to get pico while not in boot mode to show up as a USB device that we can read from.

This website goes over some libraries that can be used in python to product an oscilloscope like output, not sure if this is a live display or just produces images. This could have helpful information. There may be a way to interface with malab's plotting functions to not have to design from scratch like this example.

Piserial as used in this video may be useful for how to send the data from the pico, once serial communication is setup correctly it should more or less just be able to be received and then we can do something with it.

Conclusions/action items:

should talk with the team about if this is good to get started with and do some smaller tests to build up to a final product.



Mark RICE - Mar 07, 2025, 3:20 PM CST

Title: EEC Cap Case Brainstorming

Date: 3/7/2025

Content by: Mark

Present: Mark

Goals: Begin brainstorming and modelling a 3d printable case for the EEG Cap electronics

Content:

From 3/7 meeting and working on I2C for embedded system and the GUI being completed, my next task will be to work on a case for the entire system:

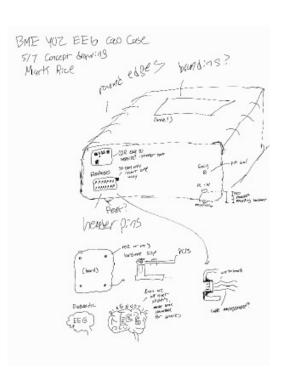
it must:

- Contain PCB
- Have IO ports for
 - gain dial
 - microUSB to pico
 - electrodes connections

For fun I would like to make it so the electrodes can be connected in only one way so it is not accidentally connected incorrectly, have branding, and potentially have braille for any wording so it could be used even by someone with limited or no vision. See connected file for design ideas.

Conclusions/action items:

I will start to model this to have ideas of what dimensions we want for the V2 board for: where header ports need to go, where the gain & pico need to be, where and what size holes should be for mounting hardware.



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Notes_250307_150608_1_.pdf (920 kB)

Mark RICE - Mar 07, 2025, 3:24 PM CST



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Case.SLDPRT (246 kB)

Mark RICE - Mar 07, 2025, 9:39 PM CST



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CaseTop.SLDPRT (121 kB)

Mark RICE - Mar 07, 2025, 9:39 PM CST



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Cap.SLDPRT (1.42 MB)

Mark RICE - Apr 04, 2025, 3:55 PM CDT

Title: Case Version 2

Date: 4/4/2025

Content by: Mark Rice

Present: Mark

Goals: design a case for the v2 circuit board.

Content:

With the new circuit board I can now update the dimensions of the concept. The main changes that need to happen are:

- Update overall width and length to fit new board layout
- · align microusb port so the pico can be plugged in
- Add holes on top to fit the 10 potentiometers
- · move the hole for the electrode headers to fit

I started a new solidworks to avoid errors associated with the concept and came up with the following design for the base, I will move on to print both parts to see how they fit before moving on to the lid.

The lid will have the holes to go gown all the way to the board for the headers and up to the top surface of the potentiometers. Something to think about is adding text to the case to make it more readable including lines to show where each channel is, what value it is roughly set at and labeling the header pins for plugging in the electrodes.

I would also like to make it braille accessible or at least tactile to make it easier to use in an environment where you cannot see.

Conclusions/action items:

Waiting for the print to finish I can see how things fit and make adjustments to the files, if this looks good I will move on to the lid.

Mark RICE - Apr 04, 2025, 3:56 PM CDT



<u>Download</u>

CaseV2L.STL (150 kB)

Mark RICE - Apr 04, 2025, 3:56 PM CDT

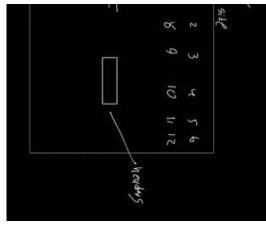


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CaseV2R_1_.STL (296 kB)

Mark RICE - Apr 04, 2025, 3:59 PM CDT





<u>Download</u>

Screenshot_20250404_155738_Samsung_Notes.jpg (46.6 kB)

Mark RICE - Apr 06, 2025, 6:14 PM CDT

Version 1 of the print did not have deep enough areas for the screws and there was not enough clearance for components underneath the circuit board. I made the whole thing a bit taller. Will see how the right part edits to see if the port needs any other updates.

This is V2.0

Mark RICE - Apr 04, 2025, 9:01 PM CDT



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20250404_205934.jpg (482 kB)

Mark RICE - Apr 04, 2025, 9:01 PM CDT



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20250404_205938.jpg (404 kB)

Mark RICE - Apr 04, 2025, 9:02 PM CDT



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CaseV2L_2_.STL (236 kB)

Mark RICE - Apr 04, 2025, 9:02 PM CDT



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CaseV2R_2_.STL (362 kB)

Mark RICE - Apr 06, 2025, 6:15 PM CDT

V2.1 update: The microusb port was a bit close, this fixes this to be a bit wider

Mark RICE - Apr 04, 2025, 11:56 PM CDT

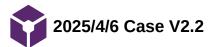


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CaseV2L_3_.STL (236 kB)



Mark RICE - Apr 04, 2025, 11:56 PM CDT



Mark RICE - Apr 06, 2025, 6:20 PM CDT

Title: Mark Rice

Date: 4/6/2025

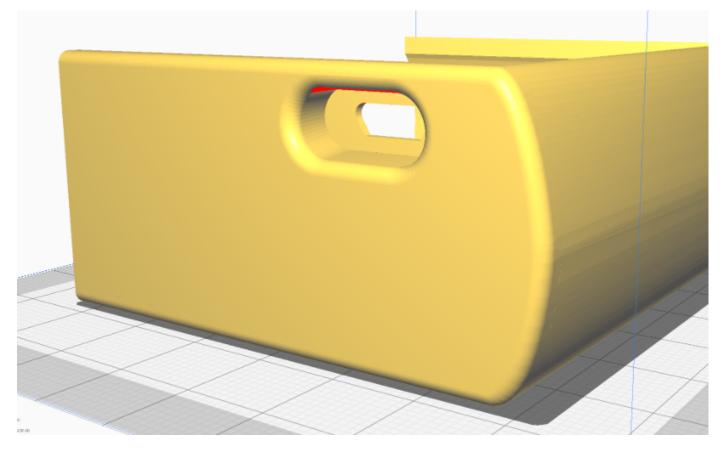
Content by: Mark Rice

Present: Mark

Goals: Update from v2.1

Content:

The main issues faced in v2.1 after printing it. is that the threads of the screw couldn't quite grip well so I gave the holes a 4 degree angle so it has something to grab onto at some point. I brought back the face where the usb plugs in and had the cut go to a flat wall to accommodate more charging cords that may not terminate directly at the perfect size. I also gave the fillet on the screws a bit longer radius since I noticed the slicer for my printer would make 2 lines of infill for the screw holes instead of just 1 for some reason. May not be necessary on other printers.



note this is just half the case, I have to print in 2 halves since my printer at home is smaller.

Conclusions/action items:

see how this version prints and if it fits well print both sides and move on to the lid.



Mark RICE - Apr 07, 2025, 7:30 PM CDT

4/7 Full bottom part of the case works well. I got started on the top part but realized either we got the wrong potentiometers or the ones we have might not work. Planning on following up with the team for this

Mark RICE - Apr 07, 2025, 7:30 PM CDT



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CaseV2L_4_.STL (259 kB)

Mark RICE - Apr 07, 2025, 7:32 PM CDT



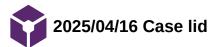
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20250407_193116.jpg (1.23 MB)



<u>Download</u>

20250407_193122.jpg (1.1 MB)



Mark RICE - Apr 16, 2025, 7:31 PM CDT

Title: Case Lid

Date: 4/16/2025

Content by: Mark Rice

Present: Mark

Goals: Design lid for case

Content:

I talked with the team and we figured out we did order the wrong potentiometers so we will not be able to test the full board with the correct potentiometers, however I made this design that should work with them. Future work could include giving lines to indicate where the potentiometers are set and testing how it fits with a fully assembled board. I considered doing a version where the left side would be lower for the header pins and potentiometers so it's a bit less awkward but then it gives up having a flat top which I also appreciate.

again it was barely too big for my printer so it is split up into 2 parts for the protype

Conclusions/action items:

I will be working on printing this to see how it fits and make design updates accordingly

Mark RICE - Apr 16, 2025, 7:30 PM CDT



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CapV2_1_.STL (711 kB)

Mark RICE - Apr 16, 2025, 7:30 PM CDT



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casev2.SLDASM (934 kB)

Mark RICE - Apr 16, 2025, 7:30 PM CDT



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EEGCase.SLDASM (975 kB)



Mark RICE - Apr 16, 2025, 7:30 PM CDT

CapV2.SLDPRT (1.03 MB)

Mark RICE - Apr 16, 2025, 7:30 PM CDT



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CapV2L_1_.STL (617 kB)

Mark RICE - Apr 16, 2025, 7:30 PM CDT



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CapV2R_1_.STL (100 kB)

Mark RICE - Apr 16, 2025, 7:30 PM CDT



Download

CapV2L.STL (617 kB)



Mark RICE - Apr 17, 2025, 3:13 PM CDT

Title: Drop Testing Protocol

Date: 4/17/2025

Content by: Mark Rice

Present: Mark

Goals: Develop a protocol for testing the case for drop testing damage.

Content:

Objective:

evaluate the durability of the EEG cap case prototype from common wear and tear use like accidental drops.

Scope

This will be done with a empty circuit board since we do not have extra components that can be damaged, further work can be considered with a full circuit prototype on board to evaluate if it can still function. For now it will look for cosmetic damage, damage to the circuitboard and how well the board stays screwed in.

Test Equipment

Calipers, phone camera for video and photo analysis, 1 3d printed prototype made from PLA for damage testing and 1 for an undamaged control, hard floor like concrete, wood, stone etc.

Drop heights

0.75 m, 1m, 1.2m or as necessary to see damage

Drop orientations (starting in this position):

Flat on base

Flat on top

Flat on front face

Flat on back face

Flat on left side

Flat on right side

One top front edge

One corner

Test procedure:

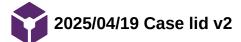
starting at 0.75m, randomly select an orientation and drop while recording with a camera. Take photos of any changes in damage, record if the damage is: cosmetic, functional and if the damage is: minor (can still be used for normal function) moderate (still works but is badly cosmetically damaged) or severe (cannot continue under normal function).

Acceptance criteria

The product is acceptable if it makes it through all orientations at all 3 heights with only receiving minor or moderate cosmetic damage, not severe damage.

Conclusions/action items:

I plan to look over this protocol with the team tomorrow and conduct the testing with Elliot as well if it looks good.



Mark RICE - Apr 19, 2025, 4:31 PM CDT

Title: Case Lid V2

Date: 4/19/2025

Content by: Mark Rice

Present: Mark

Goals: Fix alignment of potentiometers and electrode pins.

Content:

Moved potentiometers about 3mm left and 2 mm down. Moved electrode standoffs about 4 mm left and 3 mm up to fix alignment. Also added 4mm fillet to back of the clips to increase durability.

also, on the base mirrored just the loft part of the usb port so the other sides had a lowest point the lid could go down to, this could have been done cleaner in a way to not cause a little bump on the outside, instead I just filleted them to even it out a bit.

Conclusions/action items:

print these updates and prepare for poster presentation

Mark RICE - Apr 19, 2025, 4:35 PM CDT



<u>Download</u>

CapV2_1_.SLDPRT (944 kB)

Mark RICE - Apr 19, 2025, 4:35 PM CDT



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casev2_1_.SLDASM (1.31 MB)

Mark RICE - Apr 19, 2025, 4:35 PM CDT



Download

CaseV2.SLDPRT (536 kB)



Mark RICE - Apr 20, 2025, 12:58 PM CDT

Title: Drop Testing Results

Date: 4/20/2025

Content by: Mark

Present: Mark

Goals: See how the case survives common drops

Content:

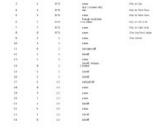
see attached data.

The case only took minor cosmetic damage from all heights meaning it should survive at least 20 countertop drops onto a hard floor, things that could be improved for later designs: keeping the screws secured better, maybe having a print that pauses to embed a nut into the hole instead of tapping it ourself and the durability of the snap tops on the lid, this may have been exasperated by me opening the lid between drops to check for damage to the circuit board. Later testing could also be done with a fully populated circuit board to be able to test if it still functionally works instead of just visual checks.

Conclusions/action items:

Send data over to Elliot for helping analysis and prepare data in a nice way for the final report and poster presentation.

Mark RICE - Apr 20, 2025, 12:59 PM CDT





Data_1_.xlsx (5.65 kB)



<u>Download</u>

1.jpg (769 kB)

Mark RICE - Apr 20, 2025, 1:02 PM CDT



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2.jpg (1.01 MB)



<u>Download</u>

control1.jpg (1.48 MB)

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control2.jpg (1.67 MB)

Mark RICE - Apr 20, 2025, 1:02 PM CDT



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control3.jpg (1.55 MB)

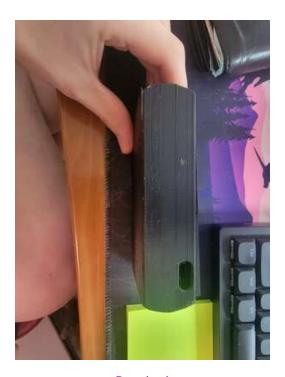
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control4.jpg (1.85 MB)

Mark RICE - Apr 20, 2025, 1:02 PM CDT

post2.jpg (646 kB)

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Mark RICE - Apr 20, 2025, 1:02 PM CDT

post1.jpg (742 kB)

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post3.jpg (979 kB)

Mark RICE - Apr 29, 2025, 3:53 PM CDT

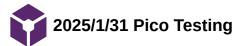
4/29: since the case is about 100g (0.1 kg), and is dropped from a height of 0.75, 1 and 1.2 it is estimated that it will hit the ground with the free fall equation and free fall speed:

s (distance travelled in freefall) = 1/2 g t², solving for t we get t = sqrt(2s/g).

I plugged this into the free fall speed equation v = g * t to get the velocity at impact dropped from a height s is g * sqrt(2s/g)

this works out so the heights 0.75, 1 and 1.2 (m) will have an impact speed of 3.8, 4.4 and 4.9 m/s.

I multiplied the mass of the case by this to get the impact force of each height as 0.38, 0.44 and 0.49 N.



Mark RICE - Jan 31, 2025, 7:30 PM CST

Title: Pico Testing

Date: 1/ 27-31 /25

Content by: Mark

Present: Mark

Goals: Documents trial and error getting pico to work.

Content:

I've been having the same issue as documented in this forum with the pico not running any code uploaded onto it.

https://forums.raspberrypi.com/viewtopic.php?t=382309

Before coming to this forum I tried running the Pico from 4 different computers running windows or linux. I tried redownloading vscode, updating driver of the storage device and using different cables and different picos.

Conclusions/action items:

Next step for troubleshooting is to update the drivers of the boot device with zadig.

🔝 Zadig	– 🗆 X
Device Options Help RP2 Boot (Interface 1)	✓ ☐ Edit
Driver (NONE) → WinUSB (v6. 1.7600.16385) → USB ID 2E8A 0003 01 ◆ Install Driver ▼ WCID ² X X X X Y Y	More Information WinUSB (libusb) libusb-win32 libusbK WinUSB (Microsoft)
1 device found.	Zadig 2.9.788

Mark RICE - Feb 03, 2025, 7:26 PM CST

Note: This method did not work. I found an example uf2 file that ran fine on the pico, but any file compiled by my pc will not work.

Mark RICE - Feb 05, 2025, 8:55 PM CST

2/5 Update

The solution to this issue was to create the project as a pico '1' project not a "pico 2" despite that the board is in fact a pico 2.

From this I used print statements to start debugging the code and slightly altered the find sample rate and change channel functions so that it spread the channel changes and reads over the whole sampling frequency in case the MUX needs time for the signal to settle before reading it. From this I hooked up LEDs to the communication pins for the MUX and lowered the sampling frequency to 1 Hz. The following video shows every second the LEDs blinking between the 10 confirmations that represent the channels for the MUX. The next step is to hook it up to the MUX and run signals into it and use print statements to understand if it can differentiate between the signals. And then adding control for the programable gain.



Download

20250205_204642.mp4 (43.1 MB)

Mark RICE - Feb 05, 2025, 8:55 PM CST

print statu()
 still (();
 still (();

Download

EEGCapEmbedded.c (5.57 kB)

Mark RICE - Feb 12, 2025, 3:01 PM CST

2/12 Update

I think I have the code working now to control the MUX and output that to the ADC onboard and have it printing the voltage read from each channel to the serial monitor. It has a strange issue where I cannot open the serial monitor at 1khz sampling rate and it only samples at about 800 Hz, I will have to look into changing the interrupt function I am using to see if I can fix this. Also on the surface mounted adapter I am using for the mux, my soldering may not be perfect so it seems like I may be leaking voltage between multiple pins, so I should test this on the actual one on the circuit board.

Mark RICE - Feb 12, 2025, 3:02 PM CST

12
ist mais()
<pre>tdis_isit_all();</pre>
<pre>shile (true) { pristf("Hello, warld(\n"); ikep_am(1000); } }</pre>
3,
sinclude "pico/std'iii.h" #include std:bool.i> #include std:bool.i> #include "tarbase std:n.h"
<pre>#iefine LED_PIN 25 // for testing #iefine Mat_converts15 to // remember of electrodes we are reading from #iefine Soft(Num_RATE 100 // inc often we want to maple is No</pre>
Constitute Conversion.Machine = $3.57 / (1 \approx 12)$; // currently unused : electric MOX_SIZE 100 // maximum number of samples we can have that we don't isolatit flast curbets[MuM_CARMOLS]; // The pass that wall Commensions with MEX
efertor 52 1967 100 52 1967 100 52 1967 100 52 1968 100 52 100 52 100 50 100 50 10000000000
<pre>wolatile set 1 = 0; // counts from 0 to NUR_Charmets set22; findSampleSate[]; set chargetSampl();</pre>
<pre>http:repearing_timer_coaltback(struct repearing_timer "t) { This is where we will collect data For testing data gpic_str(LSD_PEN, logic_str(LSD_PEN));</pre>
<pre>//certbal[] = (dsc_read() * (3.3 / e000.05)); untl2L.result = a02_read(); //pistf[] = reast * corrections.read(); //pistf["Hawsine: conduct, withing: Nr Yin", result, result * corrections.read(sci); dataget&anno((c-1)); dataget&anno((c-1));</pre>
) // TODD write the Sate somewhere
¹ Queue inplementation based on code from geeksforgeeks.org https://www.geeksforgeeks.org/queue-in-c/ ² /
Nay bring this back if we cannot deal with data suick enough but for non- igneratry to doal with data as it comes in. end instatizationse(); ioni isopary[]; indid enumene[]; indidenter[];
ist itoms[NAX_SIZE][MIM_GOUNDELS];
Download

EEGCapEmbedded_1_.c (6.14 kB)

Mark RICE - Feb 12, 2025, 3:53 PM CST

2/12

Floating channels may have lead to the "leaking" between channels. After grounding the unused inputs seems like it is now working but I may have fried the MUX so will do further tests once we can get a new chip.



Mark RICE - Feb 26, 2025, 3:45 PM CST

Mark RICE - Feb 26, 2025, 3:45 PM CST

Title: Pico I2C debugging

Date: 2/26/2025

Content by: Mark Rice

Present: Mark (Ellie & Richard for part)

Goals: Work on I2C code for embedded system controlling Digi pot

Content:

upon initially testing I2C code on the digipot, I was not reading any resistance at all between the B and W pins. I met with Ellie and Richard to debug this, the first meeting we found that there may have been a short between the VCC and VSS pins. Meeting up again on a later date in the makerspace we De-soldered this digipot and soldered a new one to a different spot and was able to read an appropriate resistance, however my I2C code would not change the resistance. Upon further inspection the I2C write blocking function would only return -1, meaning it was likely called with some information wrong or the digipot did not acknowledge the I2C line. This is something that will require additional work and debugging.

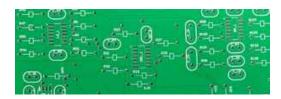
Conclusions/action items:

I plan to write a new program to debug just the I2C part of the program so it is not influenced by other parts of the program. This can be something like a channel scanner where we do not send any data and just search for a device. I may also try putting the I2C on different GPIO pins to see if that helps.

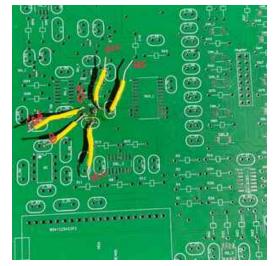
/*
if sais()
if dislocation();
if if a sais()
if if is a sais();
if if a sais();
if if is a sais();

Download

EEGCapEmbedded.c (7.78 kB)



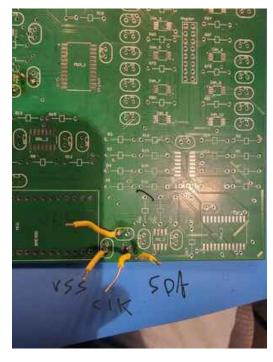
Mark RICE - Feb 26, 2025, 3:56 PM CST



Download

IMG_0183.jpg (314 kB)

Mark RICE - Feb 26, 2025, 3:56 PM CST



Download

20250225_172837.jpg (953 kB)

Mark RICE - Feb 26, 2025, 4:04 PM CST

The Following code is what I want to test hooking up just the pico to the potentiometer, note I do need to use a voltage generator to get +- 5V for VSS and VCC.

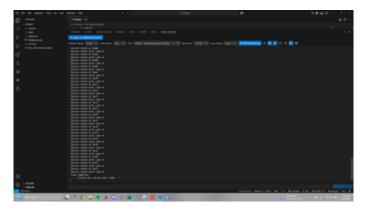
Mark RICE - Feb 26, 2025, 4:05 PM CST

eardlude #38080,h> eardlude "picovintial.h" #ardlude "bardwar#/320.h"
(7) ISX (#filed) /7 This mapple will use ISCG on GPDG (SOA) set GPDGA (SEL) runsing at 400000 /7 PLm cas be charged, see the GPDD function select table in the databaset for informatics on GPGD manipured afertum SIZ_SOAT SIZG setum SIZ_SOAT 4 // GPDG 4 SDA setum SIZ_SOA 5 // GPDG 4 SDA
ist main()
<pre>tdis_isit_all();</pre>
// I26 Initialization, Using it at 10000g. 120_1#it(I26_P0WT, 100000);
<pre>@ull.ster.twotien[ISZ.E04, 07D_UMC_ISC]; gull_ster_twotien[ISZ.E04, 07D_UMC_ISC]; gull_pill_up(ISZ.E04); gull_pill_up(ISZ.E04); gull_pill_up(ISZ.E04); seamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- esamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- esamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- esamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- esamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- esamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- esamplot/transformative/ISZ.e050 site https://jithub.com/respherypu/pic6- seamplot/transformative/ISZ.e050 site https://seamplot/transformative/ISZ.e050 site https://seamplot/transformative/</pre>
<pre>sloep_ms(2000); // Wait for USB serial to be ready pristf("I2C Scasser Starting\s");</pre>
while(3){
<pre>void scam_ibc_bus() (prist("Scheming IIC bus\v");</pre>
<pre>for (sintl_t iddr = 0; iddr < 120; iddr++) [// Try writing 0 bytes to the device; if it acksowledges, it exists sat robutt = :32write.blocksep(122.DWT, iddr, Mull, 0, false);</pre>
<pre>sr (result >= d) { printf("bevice found at BobBerry", side);) }</pre>
pristf("Scan complete.\s"); }

<u>Download</u>

I2CTest.c (1.35 kB)

Mark RICE - Feb 27, 2025, 3:32 PM CST



Download

Screenshot_3_.png (216 kB)

Mark RICE - Feb 27, 2025, 3:45 PM CST

2/27:

so when sending no data I do get a reply but I get a reply from every address it seems. This is not at all what I expected and I am confused. Will follow up with Dr Numunkar and Brandon.

The same thing happens when it is not connected at all.



Mark RICE - Mar 19, 2025, 4:07 PM CDT

Title: Code Timing Test

Date: 3/19/2025

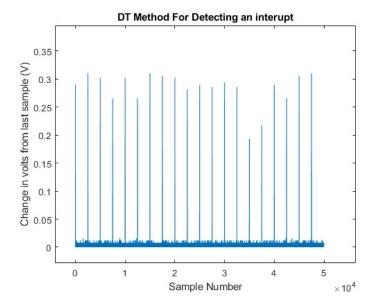
Content by: Mark Rice

Present: Mark

Goals: See how accurate the timing of the interrupts are on the pico

Content:

Using an oscilloscope I changed the LED pin to GPIO 15 and hooked up the oscilloscope to that and ground. Using that I could export a CSV of the raw data read, however it could only export a maximum of 50k data points at once despite the display seemingly showing more. Using this I got the change in voltage between each point read, I assumed any DV of > 0.2 to be a presumed interrupt that occurred. With about 20 interrupts recorded I could not get a meaningful change in interrupt time since all but 1 had the same change in time (the remaining one seemed to have a dv slightly below 0.2 so it read exactly double the magnitude of the others).



I tried exporting at a few different scales larger than this to get even number of interrupts and data points per interrupt but it seems I need to get more datapoints.

Conclusions/action items:

I should try getting just one interrupt sample per 50k data points or try to export in another format that allows more data points. We decided to avoid adding something like a print line that could tell us when an interrupt occurred because changing this in the code could add a much higher change in timing than we want.



<u>Download</u>

scope200us.csv (1.61 MB)



<u>Download</u>

scope_1ms.csv (1.56 MB)



Mark RICE - Mar 19, 2025, 4:05 PM CDT

Mark RICE - Mar 19, 2025, 4:05 PM CDT

Mark RICE - Mar 19, 2025, 4:05 PM CDT



scope_500us.csv (57.5 kB)

Mark RICE - Mar 19, 2025, 4:05 PM CDT



Download

scope_50s.csv (42.7 kB)

Mark RICE - Mar 19, 2025, 4:05 PM CDT

Mark RICE - Mar 19, 2025, 4:05 PM CDT



scope_1.csv (51.4 kB)

DT Method For Detecting an interupt 0.35 Change in volts from last sample (V) 200 cross c 0 0 1 2 3 4 5 Sample Number × 10⁴ <u>Download</u>

untitled.jpg (37.5 kB)

Mark RICE - Mar 19, 2025, 4:05 PM CDT



Download

untitled.fig (338 kB)

Mark RICE - Mar 19, 2025, 4:05 PM CDT





<u>Download</u>

TimingAproximator.m (465 B)



Download

TimingAproximator.asv (310 B)

Mark RICE - Mar 19, 2025, 7:06 PM CDT

Mark RICE - Mar 19, 2025, 4:05 PM CDT

By zooming in I can pause and resume the recording to get the width of an interrupt to about 5 sig figs, this seems like it might be easer to manually do to get random samples and saving pngs as evidence.

Sampl #	e 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Time (us)	99.988	100.40	99.992	100.62	100.00	99.992	99.988	99.988	99.992	100.62	100.40	100.40	99.988	100.40	100.40	99.988	99.988	99.992	99.988	100.40

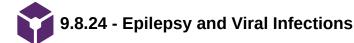
From these 20 samples we get

mean time between samples should be about 100.18 us, std 0.24 us

Could get a tool that can analyze this with more accuracy, or take samples over a longer period of time to see if it drifts on average over time. adding a trendline does show a very slight downward slope but there is verry little to no sign of statistical significance with only 20 data points

Mark Rice/Training Documentation/2025/3/19 Code Timing Test





Ellie Dingel - Sep 13, 2024, 5:58 PM CDT

Title: Epilepsy and Viral Infections

Date: 9.8.24

Content by: Ellie Dingel

Present: NA

Goals: To learn more about the background of Viral Induced Epilepsy

Reference: https://journals.sagepub.com/doi/abs/10.5698/1535-7511-14.s2.35

Content:

- Viral infections cause seizures via several pathogenetic mechanisms
 - Direct central nervous system invasion can occur
 - Metabolic compromise can occur through systemic infections like influenza

- Inflammation of direct brain tissue (encephalities) major cause seizures and increased risk epilepsy, while inflammed brain lining does not increase risk (meninges)

- HIV and AIDS cause direct CNS infection, human herpesvirus 6 may also cause infection

- 1.5 to 10 per 100,000 people experience encephalitis and seizures due to viral infections
- Japanese B most common arbovirus encephalitis

- Antiepileptic drug use includes avoiding unwanted drug interactions and toxicity to same organs, especially in immunocompromised individuals

Conclusion/Action Items:

The article gave insight into what viral infections can cause epilepsy, as well as the presence of them. This helps to aid in providing context and scope for this project. It also helps to allow individuals to see where this project could be of use. These infections should be taken into account and remembered to help provide context for the problem.



Ellie Dingel - Nov 15, 2024, 5:20 PM CST

Title: Guidelines EEG

Date: 9.15.24

Content by: Ellie Dingel

Present: NA

Goals: To learn more about some of the technical specifications that go along with taking an EEG

Reference: https://www.acns.org/pdf/guidelines/Guideline-1.pdf

Content:

- These guidelines are the minimum standard, fit for all people expect those at a very young age (pediatric EEG is more fitting)
- 1. Equipment
- Record as many channels as possible; not enough channels increases the risk for error (particularly transient activity)
- 16 channels recording mimimum number required show are producing normal / abnormal patterns
- AC wiring meet underwriters laboratories standards required hospital service; adequate grounding, all to a common point
- Usually electrical shielding patient not necessary unless proven otherwise
- Include device rhythmic, high-intensity flash stimuli
- Dig equipment conform rec guideline 8
- 2. Electrodes

- Recording electrodes free noise and drift, don't sig attenuate signals **.5-70 Hz** ; silver-silver chloride or gold disk electrodes best, other options work with amps with high impedances

- Electrodes clean to decrease noise, precautions after record patient with disease
- Needle elctrodes not recommended, if have to be used sterilize and discard; patients in coma most likely to use these
- 21 electodes and placements recommended International Federation of Clinical Neurophysuiology should be used
- 10-20 system is only one offically recommended,. should be used
- smaller number electrodes appropraite for special circumstances but not recommended
- need to ground, if other equipment grounded avoid double grounding
- Check interelectode impedance
- electrode impedance should not exceed 5kohms
- 3. Recrodings

- Montages (position of electrode pairs) designed to conform Guideline 6: proposal for standard montages to be used in clinical electroencephalography

Record name and age of pateitn, date recording, identiifi ation number, name/initals of technoogist

- calibrate beginning and end of recroding, all channels connected same pair electrodes follow at beginning, calibration is key so must be recalibrated if uncertain

- biologic calibration may be needed at times, anteroposterior derivation should be used (includes fast and alpha range patterns and eye movement activity)

- sensitiivty EEG equpment routine recording set range 5-10 uV/mm of pen deflection

Ellie Dingel/Research Notes/Biology and Physiology/9.15.24 Guidelines EEG

- Sensitivity defined ratio input voltage to pen deflection, expressed in microboltes per millimeter, commonly used sensitivity 7 uV/mm (calibration signal 50uV deflection of 7.1mm)

- Sensitibvity less 10uV/mm (like 20uV/mm) sig low-amp acitivty indeiscernible, sensitivity greater 5uV/mm normal EEG activity may overload system (cause square peaks)

- Sensitivity 5iuV/mm, to optain pen deflection 1 mm 5uV input voltage required; sensitivity increased, numerical value smaller (needs more input to move pen)

- Frequency low-pass filter no higher 1Hz, with time constant 0.16s; vital info may be lost if not in range

- high-pass filter no lower 70Hz (computer need horizontal resolution at least 1400 pixels in data display area); can distort or attenuate spikes if too high

- 60 Hz notch filter only used when other interferences fail (can distort or attenuate spikes)

- paper speed 3 cm/s or digital 10 sec/page should be utilized/ newborns can have 20 sec a page

- final calibrations should be recorded, note any changes mid recording
- baseline 20 min technically satisfactory recording
- record when eyes both open and closed
- hyperventilation should be used routinelu
- Sleep recordings should be taken
- Pateitns level consciousness should be recorded throughout
- speciral procedures for more at risk patients
- EEG for "cerebral death" requires special procedures

Conclusion/Action Items:

Further research should be conducted into the general guidelines of an eeg device. This can be implemented into the design project.

Ellie Dingel - Sep 15, 2024, 10:47 PM CDT

Constants that Summary Fectinical Requirement for Performing Chinese
Introduction
Although no single best method exists for trecording EEGs under all circumstances, the following standards are considered the minimum for the small clinical recording of EEGs. Both and a generative aspect the very source (see Ginkalance 2). Minimum Tachatard Shadards for Pakines Tachatards and the standards and the s
1. Equipment
L3 To find the derivation of EEG century, its accuracy to record sized base-only firms an any register of the acting as possible. What no fire we channels are used sized insearchy, the channess of interpretive errors increase, and, conversely, when new channels are utilized, the likelihood of such errors derawates. This is periodiarly true for trainistication of the action producing sectors were increased and the sized sector allocated base first errors producing sectors were derived by the first Additional channels of sized transcens recording are now considered the entitionen constru- te granted by a CA to entit the entit of the entit of the entit of the entit statistication of the entities of the entit of the entit of the entit of the standards registered for height learning. Adopting spreading of the priority of a channel prior statistication of the entities of the entit of the entit of the entit of the entities of statistication of the entities of the entities of the entit of the entities of the standards registered for height learning end on the installed states growers are been entities. If a the could channel are priority and the installed states growers, and such shielding are priority of the installed states growers, it is an installed and the priority. If all we could channel are priority of the priority and equiparent is not accessing, and such shielding area of the installed states growers necessary. If all we could be priority is a state of the installed states in the installed states in the installed states in the installed states and the installed states areas and the installed states are installed states in the installed states areas and the installed states a
2. Electrodes
2.3 Recording electrodes should be free of interest tosics and drift. They should not significantly atomate signable between 0.5 and 70Hz. Experimental evidence or again that is two—show featured evidence on the source of the other electrode materials and electrode pation have been effectively used especially with contemport or applicable in size high along in patience. High quality detecteds are available from sevenit manufactures and are generally preferable to home made electrodes.

Copyright © 2008 American Clinical Neurophysiology Society

Download



Ellie Dingel - Sep 20, 2024, 11:44 AM CDT

Title: EEG Technical Features

Date: 9.19.24

Content by: Ellie Dingel

Present: NA

Goals: To understand more some features of eeg circuits

Reference: https://www.bitbrain.com/blog/eeg-amplifier

Content:

Modern EEG Features Summary

- Sampling Rate : >256 Hz

- Bandwith: 0- >80 Hz (signals throughout this range; note from other source epilepsy is 3-50Hz); want to sample twice the max rate

- higher sampling more resolution, no more info
- DC coupled or high pass cutoff needed
- Resolution >= 24 bits
- Input Range: >50mV
- Input referred noise: <1 microVrms
- Common Mode Rejection Ratio (CMRR): >80dB at 50/60 Hz
- Input impedance: >100 MOhms

Conclusion:

These are just some baseline values that might help to give a sense of what is currently used to help base design off of that.

9.8.24 - The Bionode: A Closed-Loop Neuromodulation Implant

Ellie Dingel - Sep 13, 2024, 5:58 PM CDT

Title: The Bionode: A Closed-Loop Neuromodulation Implant

Date: 9.8.24

Content by: Ellie Dingel

Present: NA

Goals: To learn more about implantable devices that have been created

Reference: https://dl.acm.org/doi/fullHtml/10.1145/3301310

Content:

- Bionode custom recording device as well as stimulation
- 4 different signals can be recorded, can provide 1mA of constant current
- Gain and filtering provided at each stage
- 3 Printed circuit board assemblies bionode mainboard, powernode, feedthrough board
 - Mainboard inclused items for recording & stimulating; microcontroller, radio, antenna also included
 - Powernode provides power for mainboard
 - feedthrough board connects electrodes to main board
- Wireless Powering Transfer (WPT) provides power and space for rodent
- External base station creates wifi link between pc and bionode
- Analog front end (AFE) needed to amplify and filter signals before digitized
 - AFE has high diff input impedance, low noise, high common mode rejection ratio (CMRR), suggicient gain and bandwidth
 - gain and bandwidth specified to sense signal needed
 - AFE filter out noise typcal (nearby signal, motion, biological signals) as well as high freq rf noise injected from WPT chamber

-Bloode two paralled dual ended AFE, two stages of gain (differential and bandpass/additional gain)

- Optional passive front end filtering can help to prevent drifting dc offset voltage used for ECG, ECoG, EMG)
- First stage instrumentation amp differentially amp signal
- Second stand inverting band-pass filter with op amp
- Safety glitch system built in for releasing charge, as well as charge balance, flexible waveform generation, and constant current stimulation
- Bidirection communication occurs with the device
- Most power hungry transmit/receive radio

Conclusion/Action Items:

The bionode is a custom recording device that can be implanted for neuromodulation purposes. There are 3 main components to this assembly, and a variety of filters built into this sensor allow for it's success. Moving forward, this sensor can be referenced to help gain a better understanding of existing technology that could be used to gain ideas. It might also be helpful to reference if a road block gets put into place.



9.10.24 Circuit Design for Extraction of EEG Signals

Ellie Dingel - Sep 13, 2024, 5:59 PM CDT

Title: Circuit Design for Extraction of EEG Signals

Date: 9.10.24

Content by: Ellie Dingel

Present: NA

Reference: file:///C:/Users/ellie/Downloads/25857057.pdf

Goals: To acquire more information about circuit design for EEG signals

Content:

- EEG produced spontaneously in brain

- EEG designed circuit composed of two instrumental amplifiers, a 3 magnified 3 filtering eeg acquisition circuit, and an amplifier circuit of eeg signals based on 3 op-amps

- EEG signals low freq, weak, and have a lot of strong background noise
- Signal to noise ratio can be 1:10000
- Brain signals typicaly from .5-32Hz

pre-amplification+	⊞Gsignals ←	electroce	Pover resource	host computer
Hghpass	→ 50Hz wave	Lowp	ass	post
filtration	trapping	filtrati	on	amplification

- Circuit block diagram

- pre amplifier must have: high input impedance, high common mode rejection ratio, low noise, small non-linearity, strong anti-interference ability, appropriate freq, dynamic range

- 2 in phase parallel structure preamplifier circuit cascade
- Non shielded condition 50 Hz power freq main interference EEG signals
- set signal to cut off above 56 Hz
- post stage had to set to have zero offset voltage and drift

Conclusion/Action Items:

This team was able to build a low cost EEG machine that was able to accomplish a variety of tasks. It could be useful to take inspirational ideas from this paper if there is a point where the team stalls throughout the semester.

Ellie Dingel - Sep 12, 2024, 12:11 AM CDT

International Forum on Europy, Invitorment and Surtainable Development (JFIESD 2016)

The circuit design for extraction of electro encephalogram signals LIU Wenglang¹, QIU Lijun², FAN Qifu³, LIU Huan⁴

Ellie Dingel/Research Notes/Competing Designs/9.10.24 Circuit Design for Extraction of EEG Signals

College of control engineering, Xijing University, Xi an 710123

E-mail: 1 No-wq-66@ 163.com ; 2 glu@@tmmu.edu.on

Keywords: EEG spinals: amplitusion: Wave Bioring: Creat Design Abditiset: The design of front and spinals acquisition creation in make for extraction of EEG signals, thus making it provide to anythy, Eur, and remove the interformer of usare signal calledral form the true interaction. Alter the signal point num through both links any re-amplituder Skylphone Birstick, SNB: wave trapping, howputs Birstick, and point mylicitions, the EEG signals invertige amplituder Skylphone and no howman U <-4V, hereby meeting the mage of requirements the correstional acquisition calls along for the layer at making signal. The visualitien results show that the signal, an collected immugh the citatis, are low in discontor, and thus can be widely used in the devices for precessing EEG signals.

Introduction

Introduction EEG signals is produced spontaneously by the brain more electrical activity adating in the certrol across system archivery either activity information, through the detection and extraction of EEG signals, except for brain research, distinibuting and the structure of the signal structure of the signal structure activity is the structure of the signal structure and a scherp quantitative monitoring [1]. Bigh quarks (EEG signals can provide checked data diagnosis and activity and the signals categorized in the structure of which splitchare in circulated diagnosis and treatment of morphalopathy in the brain cognitive function research and devidement [2]. A present, the circula structure of proventifier three parallels is designed to reposed of two introversions angliter by basing and Wang [2]. Since its advantation structure is magnified the fibering EEG acquisition circuit [4], Yourning Sandosignal a amplifier circuit of EEG signals haved on three op-sing [1].

op-amp[1].

Clearly display EG signal is signal of low frequency, weak, and strong noise background, which is an unstable and more signal isoscible to complex Bit [5]. It is between 10 V – 100 V, while the input signal to make the isoscible isologic brain detection signal buyency of EEG signals is weat of Bits. It is signal isoscible isologic brain detection with a weight of the spectra signal is made is signal production of the spectra signal buyency of EEG signals is were difficult. When the spectra buyency being the distribution with weight any spectra signal buyency is being and the spectra signal buyency and analysis of EEG signals by conflowope or USB interface in the compare. In resolution with objective of the solid get detection and estimation of EEG signals bused in the compare. In relationships, we doing the effortive detection and estimation of EEG signals bused in the compare.

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25857057.pdf (1.43 MB)



Ellie Dingel - Sep 20, 2024, 11:06 AM CDT

Title: Epileptic Seizure Detection

Date: 9.19.24

Content by: Ellie Dingel

Present: NA

Goals: To understand more about the proper guidelines for Seizure Detection

Reference: https://www-sciencedirect-com.ezproxy.library.wisc.edu/science/article/pii/S1059131117303795

Content:

- Used Wavelet packet transform (WPT) to analyze data
- Daubechie wavelet DB4 used as mother wavelet
- most seizure activity occurs 3-30 Hz, not uncommon to see 40-50Hz
- majority seizures, rhythmic seizure components bigger amp pre-seizure background
- background estimated for 240 s, followed by delayed 120 s for onset of seizure

$$IP\left(b
ight)=\sum_{f=f_{1}^{b}}^{f_{2}^{b}}\mathrm{PSD}\left(f
ight),$$

- power spectral density describes distribution signal power in frequency domain (shows strength of energy as a function of frequency), computed by Welchs method (divides data overlapping segments, computes modified periodogram, and averages periodogram)

Pattern Match Regularity Statistic (PMRS)

- taking data from entropy, approximate entropy quantify complexity and creation information; estimated similarity use equation below, where r is threshold value

$$\max_{0\leq k\leq m-1}\left|x\left(i+k
ight)-x\left(j+k
ight)
ight|\leq r,$$

- to be added to series, have to have vectors in the same range and they have to pattern match one another (instead of value)

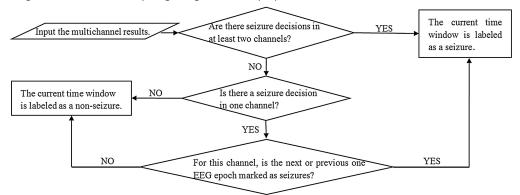
- During epileptic seizure, complexity EEG time series decreases, PMRS quantifies regularity EEG data detecting seizure activities

- Can use extreme Learning machine (ELM) additionally emphasis on minority classes (seizures)

- Can use single hidden layer feedforward neural network (SLFN) with 40 hidden neurons, sigmoid function as hidden layer activation function (transforms input into output in the neural network)

- output two values, either (1,0) or (0,q) for seizure or non-seizure
- actual values not this, moving average filter smooths decision variable
- * this study used 6 channels
- collar technique to make sure catches all of seizure (examines both seizes of seizure event)
- flow diagram for seizures

Ellie Dingel/Research Notes/Competing Designs/9.19.24 Epileptic Seizure Dectection



- EEG data processed in matlab
- Sensitivity ratio true pos over number seizure epohcs EEG experts
- Specificity ratio ture neg over total num non-seizure epoch marked EEG experts
- only one undecteded seizure in 21 patients
- G mean (square root sensitivity and specificity) is 93.96%, sensitivity 97.73%, false alarm .37/hour

Conclusion/Action Items:

Lots of information regarding the precise quantities used to create the circuit. Continue to research other designs.



Ellie Dingel - Sep 20, 2024, 11:06 AM CDT

Title: Two Electrode EEG Amplified for BCI (Brain Computer Interface)

Date: 9.19.24

Content by: Ellie Dingel

Present: NA

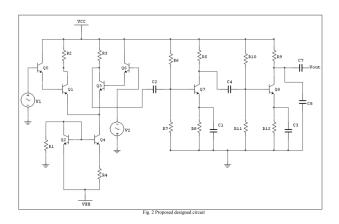
Goals: To understand more about the gain for EEG Circuits

Reference: https://core.ac.uk/download/pdf/162012173.pdf

Content:

- EEG signal 1u to 100mV, high gain amplifier of 10,000-1,000,000
- in portable equipment 50Hz notch filter and isolation can be avoided
- AC couple to reject common mode
- Transistors wanted for amplification of the circuit

Circuit design



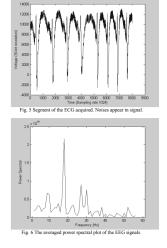
- differential amplifier used to amplify signal between two electrodes

- Common emitter amplifier set to 20; differential amplifier 50, CE amp number can change depending on what is needed

- Want as large of a capacitor as possible (close 1 Farad), but increases size of the capacitor, so some trade off there
- When circuit operated with real people had gain 86 dB (20,000) [dif amp with 2 gain amplifier units]
- This circuit bandwidth was 1-100 Hz

Data from EEG signal





Amplifier specifications

TABLE 1

AMPLIFIER'S SPECIFICATION

Input impedance	46.8Mohm		
Bandwidth	0.8-100Hz (important clinical signal fall in		
	range 1-30Hz)		
CMRR	87.6 (above the minimum required, 80dB)		
Min. input	+- 2.5uV (with 3 gain amplifier units)		
Max. input	+- 30mV (with 1 gain amplifier units)		
Power consumption	0.68mA * 10V = 6.8mW		
per channel			

Conclusion:

The circuit created had some successful acquisition of signal, however noisy. Continue to investigate other sources.



Ellie Dingel - Sep 20, 2024, 12:07 PM CDT

Title: Nonlinear Measures of Brain Rhythms

Date: 9.20.24

Content by: Ellie Dingel

Present: NA

Goals: To understand more about the gain for EEG Circuits

Reference: <u>https://bmcmedinformdecismak.biomedcentral.com/articles/10.1186/s12911-021-01631-6#:~:text=The%20results%20demonstrate%20that%20KFD,used%20to%20analyze%20EEG%20data.</u>

Content:

- KFD highest ranking feature; Katz fractal dimension method
- Beta and theta sub-bands most important (theta 3.5-7.5 Hz, beta 13-30 Hz)
- Applied to online dataset
- sampling: duration 23.6 sec and 173.61Hz sampling frequency
- 5 collections with different letters, each category 100 single channel EEG
- A 5 normal subjects 10-20 electrode system, awake and relaxed, eyes open
- B 5 normal subjects 10-20 electrode system, awake and relaxed, eyes closed
- C 5 patients seizure free intervals epileptogenic zone
- D hippocampal formation opposite hemisphere
- E signals with seizure activity

- Katz method: normalized formula calculation fractal dimension, can be obtained by taking log base 10 of u and dividing by b

- U is whole length of curve by summing distances consecutive points
- b how far apart first point and farthest point of curve
- both normalized by "m", mean distance successive spots

$$K = rac{\log_{10}(U/m)}{\log_{10}(b/m)} \mathop{=}\limits^{n=U/m} rac{\log_{10}(n)}{\log_{10}\left(rac{b}{U}
ight) + \log_{10}(n)}$$

Higuchi fractal dimension (HFD)

- average length for all temporal signals (Af), mean value computed for every novel time signal (novel temporal signals denoted as p; temporal signals denoted as T)

- HFD derived by gradient of straight line fitting points

$$A_f(p) = \left\{ \left(\sum_{j=1}^{\lfloor \frac{\gamma-f}{p} \rfloor} |T(f+jp) - T(f+(j-1),p)| \right) \frac{\gamma-1}{\lfloor \frac{\gamma-f}{p} \rfloor, p} \right\} \middle/ p$$

$$A(p) = rac{1}{p} imes \sum_{f=1}^p A_f(p) \; .$$

Top ranked features for classification problems

Sub-sets	Rank					
	1	2	3	4	5	
ABCD/E	KFD	KFD	KFD	KFD	HFD _{kmax=45}	
	(Theta)	(Beta)	(Delta)	(Alpha)	(Beta)	
AB/CD/E	KFD	KFD	HFD _{kmax=30}	HFD _{kmax=45}	KFD	
	(Theta)	(Beta)	(Original Signal)	(Original Signal)	(Delta)	
A/D/E	KFD	KFD	HFD _{kmax=30}	HFD _{kmax=45}	KFD	
	(Beta)	(Theta)	(Original Signal)	(Original Signal)	(Alpha)	
A/E	KFD (Theta)	KFD (Beta)	KFD (Alpha)	KFD (Delta)	KFD (Original Signal)	
D/E	KFD	KFD	KFD	Hurst Exponent	KFD	
	(Beta)	(Theta)	(Alpha)	(Beta)	(Delta)	

Conclusion:

Continue investigation into various EEG models to allow for more hollistic picture.



Mark RICE - Sep 20, 2024, 2:20 PM CDT

Title: Nonlinear Measures of Brain Rhythms

Date: 9.20.24

Content by: Ellie Dingel

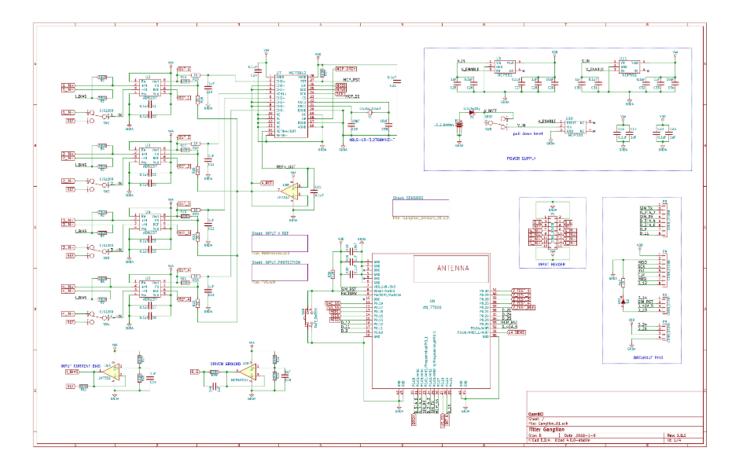
Present: NA

Goals: To research Ganglion Board

Reference: <u>https://shop.openbci.com/products/ganglion-board?srsltid=AfmBOoqScMMvShq4YgG8shccITk_PPbuyVfkuy-Z-OQHF3qaOJTkP5P1</u>

Content:

- Ganglion Board is option for for product
- 4 channels
- sampled at 200 Hz
- wireless (w battery)



Comments

Amit Nimunkar

Sep 29, 2024, 9:40 AM CDT

Please add some description for different sections of these schematics, what those are and what is the gain, bandwidth and such for this circuit.



Ellie Dingel - Sep 27, 2024, 11:15 AM CDT

Title: Low Cost EEG

Date: 9.23.24

Content by: Ellie Dingel

Present: NA

Goals: Gain a better understanding of Circuit

Content:

- RFI at beginning to attenuate radio frequency
- can form balanced bridge with resistors and capacitors
- Instrumental amp has approximately gain 11
- High pass filter around 2 hz
- Main amplifier with cutoff frequency around 150 hz
- Also includes a bandpass filter to help with frequencies (90/110 hz to .1/.3 hz)
- Variable gain also included to have additional signal amplification

Conclusion:

Take information to help create final circuit.

9.16.24 IEEE Recommended Practice EEG



Ellie Dingel - Sep 20, 2024, 12:22 PM CDT

Title: IEEE Recommended Practice EEG

Date: 9.16.24

Content by: Ellie Dingel

Present: NA

Goals: To understand guidelines IEEE

Reference: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10186304

Content:

- inteded use needs to be disclosed
- Has to be sold as a medical device
- System must adhere to IEC 60601-1 Safet and Essential Performance Standard

- must categorize information by components, document, 4 components are: electrode/sensor, acquitision, software, computer

- Electrode useage:
- Must list lifetime electrode, may be duty cycle or usage time
- Electrode performance bandwidth should be listen
- Polarization rate should be given
- Long term stability listed, reported max single usage time
- Must properly clean, products avoided should be listen
- Must be biocompabtilbe, ISO 10993
- Placement documented by system
- Must check impedence

Acquisition

-All items that must be specified and labeled

Amplifier Specifications	Frequency specifications	Analog to Digital Conversion
Input impedance	Magnitude response	Number of bits, number of channels, and type input/output channel
DC/AC coupling (time constant if ac coupled)	Phase response	Sampling rate
Noise/sensitivity (RMS and/or peak-peak voltage, given bandwidth or application, noise spectrum)	Corner frequency / frequencies	Anti-aliasing filter specification
Signal input range	Decay and rolloff	Resolution, quantization error, and/or least-sig bit size (eg performance over temperature, hysteresis, etc.)
Signal output range	Decibel (dB) attenuation in stopband	ADC technique
Ground type (active/not) or direct reference line noise		Channel-to-channel isolation and digital channel
CMRR		
Gain		
Bandwidth		
Supply voltage/current consumption		
Impedance checking specifications (stimulus, measurement time/duration, absolute accuracy, relative accuracy)		
Amplification		

Software

- Document software

- frequency processing; provision display raw signal, band of interest (if selected) should have process, minimum 2 frequency bands selectable for processing

- Characterization of data can include: amp, power values, ratio, derivation, coherence values, phase-to-phase changes, other

- Software should record: time day start, filter setting, electrode placement and changes, frequency band or filter change, processing mode changes, other tech amplifier control settings

Conclusion:

There are lots of technical specifications that need to be specified when making EEG. Make sure to refer to document to have all specifications.



Ellie Dingel - Feb 12, 2025, 11:51 AM CST

Title: Circuit Problem Solving

Date: 1.27.25

Content by: Ellie Dingel

Present: Richard

Goals: To figure out why the circuit isn't working as expected

Content:

Circuit was taken to the makerspace to figure out why it isn't working. It was discovered that there were multiple faulty traces by using a multimeter. These traces were fixed by soldering a wire into both sides. Other boards did not have the same issue with these traces, so it is a printing error. Will continue to check traces as needed.

Conclusion:

The board needs to continue to be worked on. There were multiple faulty traces which were fixed with a wire. Before the next board is utilized, traces should be analyzed. Alternatively, this board should be sourced from somewhere else.



Ellie Dingel - Feb 12, 2025, 11:53 AM CST

Title: Circuit Problem Solving

Date: 1.29.25

Content by: Ellie Dingel

Present: Richard

Goals: To populate another circuit channel for testing

Content:

Circuit was taken to the makerspace to populate a second channel. While this channel can't be tested immediately, it will allow for testing following the completion of the embedded system coding. This will help to speed up the process of circuit creation.

Conclusion:

The board needs to continue to be worked on, mainly focusing on the embedded system. Once testing can be conducted, the team can begin to design the second version of this board, which will need to be completed prior to spring break.



Ellie Dingel - May 04, 2025, 6:50 PM CDT

Title: Circuit Problem Solving

Date: 2.12.25

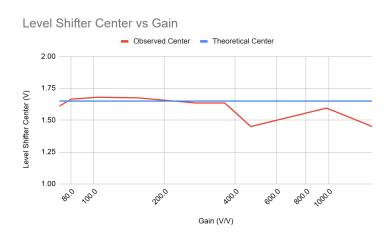
Content by: Ellie Dingel

Present: Richard

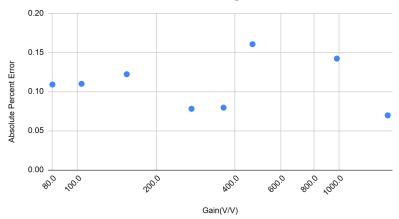
Goals: To verify the gain on the circuit

Content:

Circuit was taken to the makerspace and the gain was tested. Through the data, the following graphs were obtained. This helped to prove that the gain is within acceptable tolerances for the circuit, as stated in the PDS.

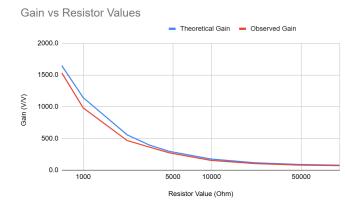


Theoritical Gain Overall and Percentage Gain Diff



Ellie Dingel/Design Ideas/2.12.25 Circuit Gain Verification

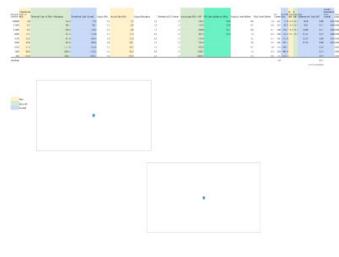
120 of 178



Conclusion:

This gain is acceptable. This data should be put within our final report and shared with the team.

Ellie Dingel - Feb 14, 2025, 2:04 PM CST



Download

Testing_Circuit_for_Gain_.xlsx (41.1 kB)



Ellie Dingel - Apr 05, 2025, 8:18 PM CDT

Title: Digikey Order

Date: 2.1225

Content by: Ellie

Present: Ellie

Goals: Digikey order to gain additional parts

Content:

The team needed more parts from digikey in order to complete testing. Thus I put together a list of parts that needed to be ordered. This list has been sent to the client and the parts will be utilized once they arrive. Having these parts will allow for more testing and development.

List : https://www.digikey.com/en/mylists/list/QQDKRW1KW0

Conclusion:

Ensure that these products get appropriately delivered to the team.



Ellie Dingel - Apr 05, 2025, 7:51 PM CDT

Title: Common Mode Signal

Date: 2/19

Content by: Ellie

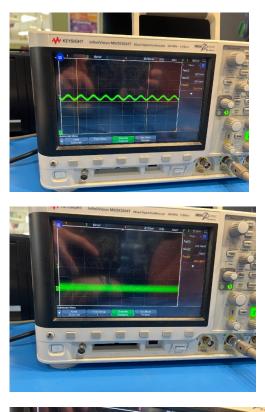
Present: Ellie, Richard

Goals: Test to see the common mode signal

Content:

input signal: 200 mV Peak to peak, 1.7V offset, 20Hz.

The two inputs are identical in order to ensure that the common mode signal is acquired. The figures below demonstrate the steps that took place during testing. We tested the output at the voltage follower and instrumentation amplifier. We were able to confirm that the common mode is being rejected as expected. The difference of signals can be seen in the last image.





Ellie Dingel/Design Ideas/2.19.25 Common Mode Signal

Conclusions/action items:

The common mode is working properly, so continue testing on other components. Make sure to incorporate this into the second version of the circuit.

Ellie Dingel - Apr 05, 2025, 7:56 PM CDT

Title: Testing of the Rheostat

Date: 2.26.25

Content by: Ellie

Present: Ellie, Mark, Richard

Goals: Figure out why the digital rheostat isn't working

Content:

We attempted to test the circuit, but were unsuccessful. We noted that the Vss and Vcc pins can be easily shorted and cause damage, which caused us to order more. I have put together a digikey order to accomplish this.

The rheostat, once turned on, gave a value of 50kOhms. However, we were not able to change this value. It was sent to 50Kohms no matter what. The code was rechecked, as was the communication, however the issue could not be located. Testing will resume another day to try and address the issue.

The rest of the circuit was tested using this 50kohm value, and it was proved to be successful.

Conclusion:

We will need to figure out the error that is causing issues. Once this is tackled, we can test how effective the MUX is and continue to V2 of the circuit.



3.4.25 Circuit Version two schematic

Ellie Dingel - Apr 05, 2025, 8:04 PM CDT

Title: Testing of the Rheostat

Date: 3.4.25

Content by: Ellie

Present: Ellie

Goals: Begin the circuit Schematic in Altium

Content:

The circuit schematic was started in altium. Today, the focus was on reworking the instrumentation amplifier, specifically with application of the DRL. The past version of this circuit was not correct, however the team was able to breadboard the improved design. This design was then implemented into the schematic today. The new design has a different order of resistors and allows the common mode rejection to occur. This schematic will continue to make the second board.

Conclusion:

Continue to work on the circuit schematic to have a final design available to order prior to spring break.



Ellie Dingel - Apr 05, 2025, 8:07 PM CDT

Title: Embedded System Testing

Date: 3.5.25

Content by: Ellie

Present: Ellie, Richard

Goals: Testing of the MUX

Content:

We were able to attain signals from channel one and three in the first configuration (parallel). The other channels showed a different signal, which meant that the signals acquired were not a fluke. The other configuration showed the same display as channel one, which was confusing. This issue will be debugged in the future after the rheostat is figured out.

Conclusions/action items:

We will need to continue to debug the rheostat and provide additional testing to the circuit.



Ellie Dingel - May 04, 2025, 6:51 PM CDT

Title: CMRR and SNR Testing

Date: 3.13.25

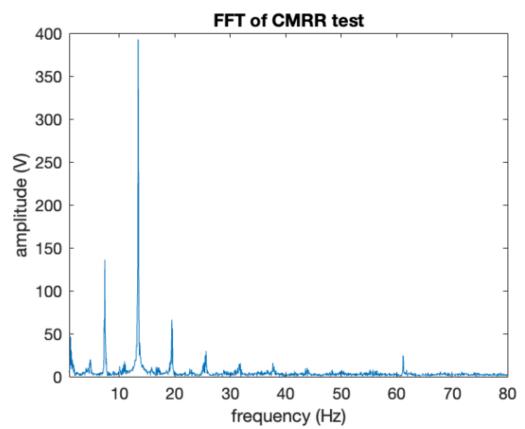
Content by: Ellie, Richard

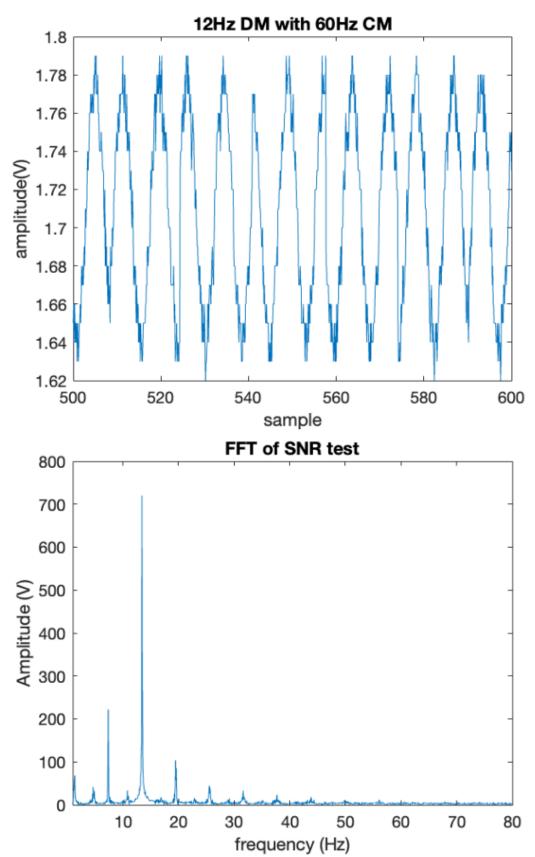
Present: Ellie, Richard

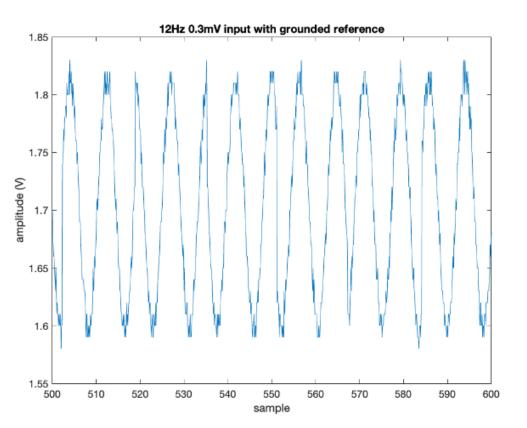
Goals: Provide more insight into CMRR and SNR

Content:

CMRR was conducted with a 120 mV signal at 12 Hz and a 20mV signal at 60 Hz. The CMRR was 2.65V/V, which is 8.5dB. For the SNR, there was a .3mV signal at 12 Hz untilized, which was tested against ground. The SNR was 3740V/V, which is 71.5dB. The graphs generated below by richard demonstrate the results that we achieved. These results are adequate given the scope of the project, and we will be utilized the configuration tested (parallel).







conclusion:

As this has given adequate results, we intent to begin crafting V2 of the circuit board. These results are deemed appropriate for our usage.

Ellie Dingel - Mar 14, 2025, 11:57 AM CDT

Title: Outreach Contact

Date: 3.14.25

Content by: Ellie Dingel

Present: N/A

Goals: To set up an outreach event for the team to participate in

Content:

The library was contacted in order to set up an outreach event. This contact has been ongoing in order to organize an event. They asked for a description of the event, which I have included information on below. The team will be informed and we will refine this as needed.

· How would you like to use the space?

We would like to use the space to host an outreach event for the community surrounding biomedical engineering. The target audience for this event will be children from K-12.We plan to give a brief background presentation surrounding how biomedical engineering operates in society. Then, we would perform a hands-on activity with the attendees to get them thinking about how to apply the principles we discussed.

· How many guests do you estimate will attend?

• Do you plan to have food/beverage?

No

• Do you need any AV?

We plan on having a presentation, so having a screen or device to project to would be wonderful. We also have a projector that we can use if a device is not available, as long as we have a blank wall.

• Is there a time/date you are hoping to book?

We were hoping to book a time in early April.

• Who is invited to your program, and how are they invited?

Everyone is invited! We can send out an email to some local schools and contact individuals that we have connections to.

• Is your program only for members?

No, this program is for anyone and everyone who wants to attend!

• What is the charge to attend your program?

It is free

Conclusion:

The outreach event should be set up as soon as possible to ensure everything can be organized effectively. We also want to make sure that we can complete the event before the deadline.



Ellie Dingel - Mar 21, 2025, 11:00 AM CDT

Title: Circuit Board Version 2

Date: 3.21.25

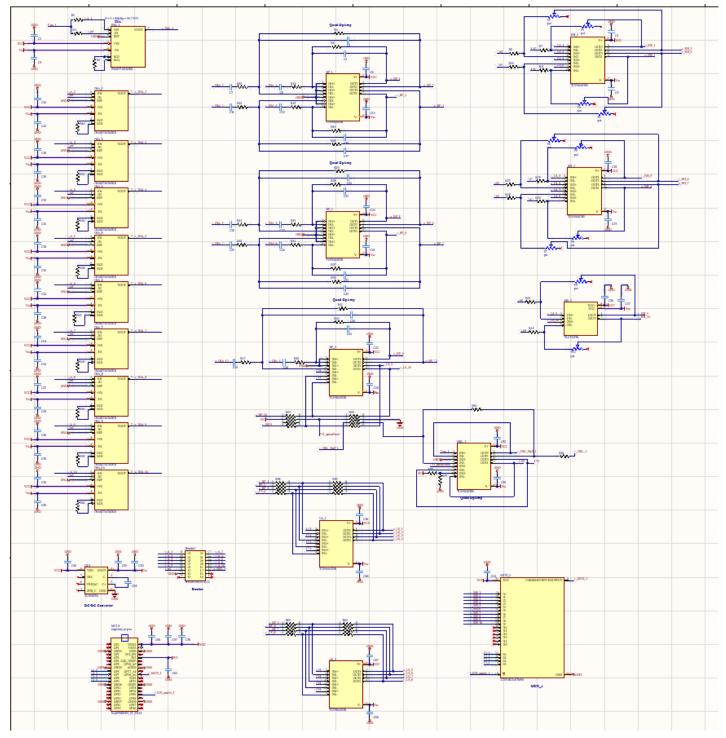
Content by: Ellie Dingel

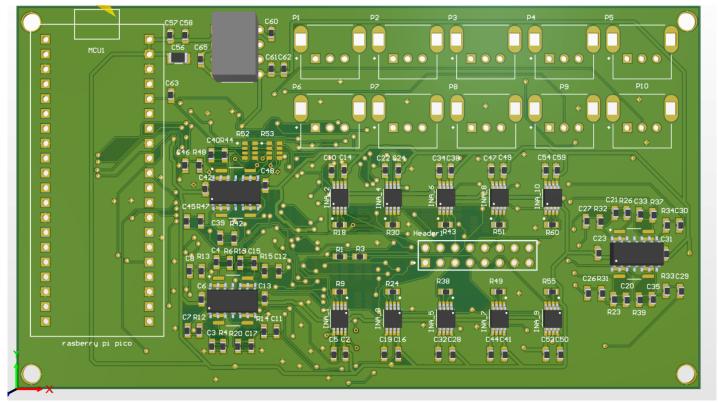
Present: N/A

Goals: To create a second circuit board with an improved design

Content:

The second version of our circuit board was designed. We switched all through hole components to surface mount ones. We were able to identify errors with the driven right leg configuration, which were fixed for this version of the board. We also switched out our digital potentiometer for a manual one. We changed some resistors to be in pad form to condense the board. Finally, we have one design for all 10 channels to help ensure more consistent results.

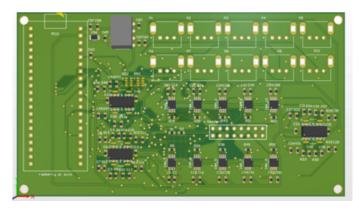




Conclusion:

The board will need to be soldered once it arrives. We should conduct testing to confirm that all of our calculations are correct. Then, we will perform testing on an individual.

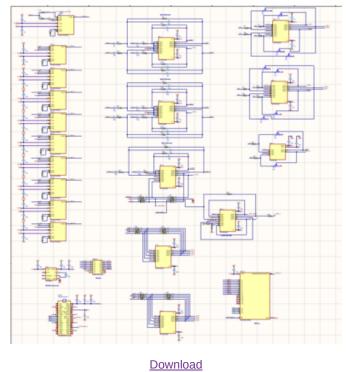
Ellie Dingel - Mar 21, 2025, 11:01 AM CDT



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Screenshot_2025-03-21_105314.png (481 kB)

Ellie Dingel - Mar 21, 2025, 11:01 AM CDT



Screenshot_2025-03-21_105355.png (127 kB)

Ellie Dingel - Apr 05, 2025, 8:27 PM CDT

Title: Digikey Order

Date: 3.21.25

Content by: Ellie

Present: Ellie

Goals: Digikey order to get parts for version 2 of the circuit

Content:

The team needed the components to populate V2 of the circuit board. Thus I put together a list of parts that needed to be ordered. This list has been sent to the client and the parts will be utilized once they arrive. Having these parts will allow for more testing and development.

List : https://www.digikey.com/en/mylists/list/RHHWVU2KGP

Conclusion:

Ensure that these products get appropriately delivered to the team and the circuit board gets populated appropriately.

Ellie Dingel - Apr 05, 2025, 8:30 PM CDT

Title: Outreach Event

Date: 3.31.25

Content by: Ellie

Present: Ellie

Goals: Outreach Event

Content:

I have scheduled the outreach event of the team. We will be going to a local elementary school and interacting with kids. This will occur from 10:20-11:10am on Wednesday, April 9. The teacher is Deb Rumpf. This class has 24 students, and we plan to run the hand prosethic activity with them. I have been corresponding with the teacher to ensure that this event runs smoothly.

Conclusion:

Attend the outreach event and make sure that everyone has a good time participating!



Ellie Dingel - Apr 10, 2025, 1:56 AM CDT

Title: Circuit Component Delay Contact

Date: 4.7.2025

Content by: Ellie

Present: Ellie

Goals: Contact Client to figure out why circuit components are delayed

Content:

Team had not yet received circuit components, despite ordering two weeks prior. After reaching out to client, found out that the op amps that were ordered were out of stock. This caused the entire order to be delayed. The circuit components, however, are now on their way and expected to be here within the next week.

Conclusion:

Ensure that the team can acquire the op amps and find replacements if unable to.



Ellie Dingel - Apr 10, 2025, 1:53 AM CDT

Title: EKG Acquisition

Date: 4.10.25

Content by: Ellie

Present: Ellie, Richard

Goals: To acquire EKG

Content:

We sat down to acquire EKG on GUI in order to have data. Ran into problems initially as the gain was not high enough. After switching out resistor, had correct gain but lots of noise issues. Decided to switch subjects from Ellie to Richard, which seemed to improve the quality. We were able to acquire a signal within the GUI, so should be able to process that data to provide visualization. This can help give us some data to compare to when we get the second version working. Below is an image of the data on the oscilloscope.



Conclusion:

Analyze the data in order to have a comparison metric for version two of the circuitry.

Ellie Dingel - Apr 18, 2025, 11:38 AM CDT

Title: PCB Testing (V2)

Date: 4.14.2025

Content by: Ellie

Present: Ellie, Richard

Goals: Test the PCB to see how it works

Content:

We got the new PCB board in. We soldered components to the first signal trace so that testing can be preformed in the future. There are stilla few components that are on their way, which should arrive soon.

Conclusion:

We should test the board and see if the signal acquired is appropriate.

Ellie Dingel - May 02, 2025, 11:45 AM CDT

Title: V2 Testing

Date: 4.18.2025

Content by: Ellie

Present: Ellie, Richard

Goals: Further Test V2 of the design

Content:

We got the pcb and continued to test the design. We were able to multiplex channels to see the output of them on the GUI, which was good for visualization purposes. This also meant that we were able to plug in the potentiometers and see exactly how they functioned. It was good to be able to see how easily the gain of the circuit can change with the twist of a knob. While we had to terminate earlier than we would have liked due to operational hours, we plan to continue to test the board in the near future.

Conclusion:

The board should continue to be tested to gain more precise specifications.

4.21.25 Final Testing

Ellie Dingel - May 02, 2025, 11:54 AM CDT

Title: Final Testing

Date: 4.21.2025

Content by: Ellie

Present: Ellie, Richard

Goals: Conclude testing on the circuit design

Content:

We were able to conduct lots of testing within this session. This testing includes:

1. Testing the evoked potential. We placed electrodes on the center of the forehead (in accordance with the 10-20 system), and then placed ground on the right mastoid and reference on the left mastoid. We were able to observe a signal which occurred both through blinking, as well as moving the eyes from left to right.

2. The driven right leg was tested. We were able to accomplish this by hooking up channel 1, both with the driven right leg connected and disconnected. The soldering iron was brought close to the circuit to cause interference. From observation, there was no difference. This will be analyzed further to see if there was any difference following the processing of the data.

3. The channels were fully populated, which helped to increase the accuracy and decrease the noise of the circuit.

4. Recording that occurred from all 10 channels at the same time. This helped to ensure that the mux was functioning properly and gave us confidence in our design.

Conclusion:

The results gathered from this testing data should be further processed and analyzed to draw conclusions from, as well as place on our final poster.

Ellie Dingel/Design Ideas/4.22.25 Data Analysis



Ellie Dingel - May 04, 2025, 7:05 PM CDT

Title: Data Analysis

Date: 4.22.2025

Content by: Ellie

Present: Ellie

Goals: Analyze the Data that was acquired during testing.

Content:

Got the results from testing both channel 1 and 2 at three different frequencies. These three frequencies should be analyzed to determine the CMRR for each of these. Coded in matlab to display the graphs for both the CM and the DM throughout the data. Using an FFT, also was able to acquire the CMRR for each of these three frequencies for the two different channels. The calculated values and the graphs are inserted below.

CHL 17 .34AR 64 39aB 68.11aB 65.86 dB 1042 64.43dR 65.51dB

Conclusion:

Should be placed on the poster to present the data.



Richard YANG - Feb 20, 2025, 3:57 PM CST

Title: common mode signal verification

Date: 2/19

Content by: Richard

Present: Richard, Ellie

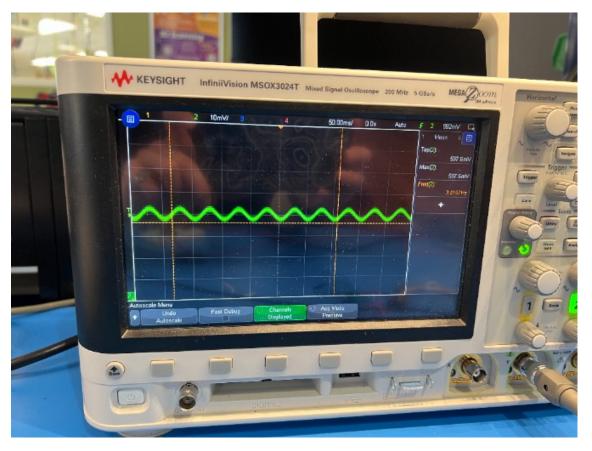
Goals: verify that we can obtain the common mode signal with the circuit proposed in 2/14.

Content:

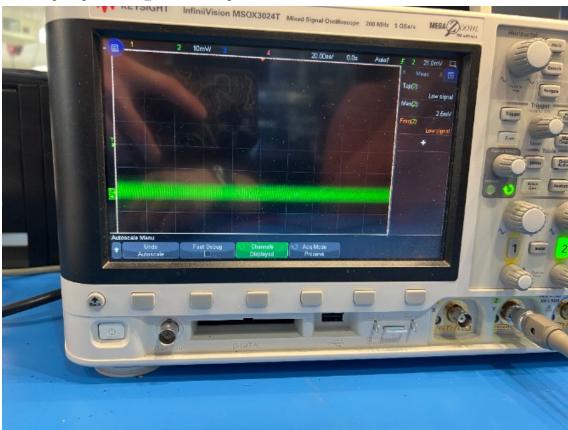
input signal: 200 mV PtP, 1.7V offset, 20Hz.

The two inputs are identical.

First figure is the common mode signal observed at the output of the voltage follower. The amplitude is smaller than expected because the input impedance to the opamp is 1MOhm.



This figure is the output observed at instrumentation amplifier. All common mode signals are rejected.

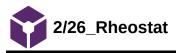


This figure is obtained by using two different inputs: 150 and 200 mV, as inputs. This is observed at the ouput of the voltage follower.



Conclusions/action items:

Include this correction in v2. Work with Mark to test the MUX and Rheostat.



Title: Rheostat testing

Date: 2/26

Content by: Richard

Present: Richard, Ellie, Mark

Goals: debug digital rheostat

Content:

Note, be careful with the Vss and Vcc pins. The rheostat can be easily damaged if these two pins are shorted, which is very easy to do.

After rectifing the soldering, the rheostat is correctly initialized the 50kOhm(48k Observed).

However, the I2C function call continues to return -1 and the resistance cannot be set by the microcontroller.

Things already tried but did not resolve the problem:

- 1. message buffer type, this should be a pointer to uint8
- 2. address, this should left shifted by 1 bit, since we are putting a 7 bit address into a 8 bit buffer.
- 3. Payload. This should be two bytes, with a command followed by data.

Possible error not tested:

- 1. clock signal correctness
- 2. Timing correctness

Current suspicion is that the slave did not receive the command correctly; thus, the ack bit was not received by the MCU. However, the issue could also occur on the MCU side where the command was never sent in the first place.

Conclusions/action items:

Obtain logic analyzer from Brandon to see the output from the SCK and SDK pins.



Richard YANG - Mar 05, 2025, 3:44 PM CST

Title: GUI

Date: 3/4

Content by: Richard

Present: NA

Goals: develop the GUI for ease of testing

Content:

all 10 channels are displayed in the GUI (assuming the MCU sends the correct data).

Max GUI sampling rate is 25Hz. We need to investigate if this is the maximum rate the .py file is receiving the data or the maximum that the MCU is sampling data.

Conclusions/action items:

debug the GUI according to the above description



3/5_briefAnalysisofTestingResult

Richard YANG - Mar 05, 2025, 6:26 PM CST

Title: brief analysis

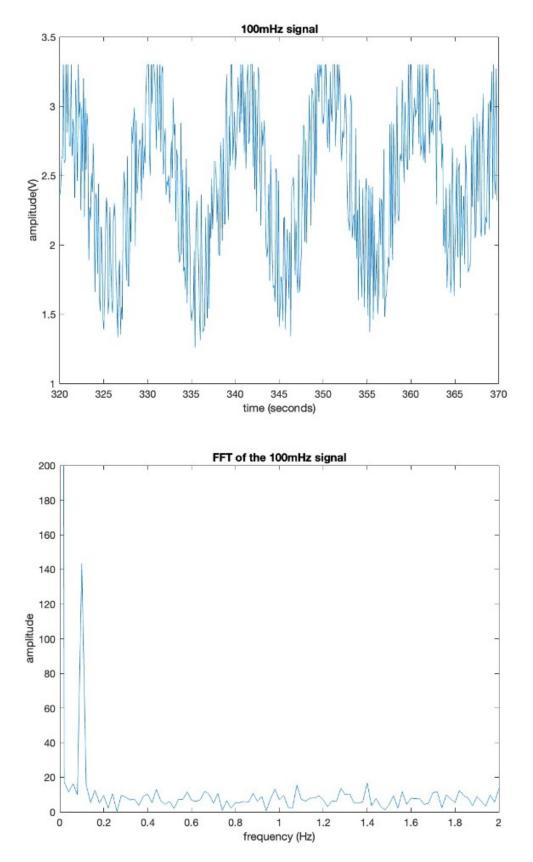
Date: 3/5

Content by: Richard

Present:

Goals: briefly visualize the signal and calculate the fft. This is just a sanity check.

Content:



As expected, we see two spikes: dc and 0.1Hz.

Conclusions/action items:



Richard YANG - Mar 06, 2025, 5:16 PM CST

Title: fixing race condition in embedded

Date: 3/6

Content by: Richard

Present: NA

Goals: optimize data transmission

Content:

previous implementation involved two asychronous threads: sampling and sending data. This creates race conditions when the two threads trys to access the same registers at the same time. Furthermore, we cannot gurantee that the data is the register is not stale.

Improved implementation: we send the data in batches to reduce overhead. This is done in the callback function. Whenever a batch is full, we then set a global flag for the main function to send the data over. While this is happending, the sampler can start filling up a second batch. The new implementation also involves a lock to protect the critical sections.

a 20 microsecond sleep is also implemented at the end of MUX switch to waist for the system to stabilize.

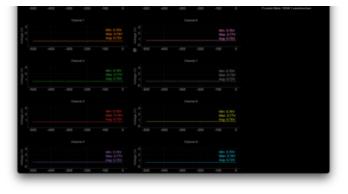


Conclusions/action items:

Pay attention to write speed. Current estimate is 51 bytes per 10 samples meaning 51KB/s.

Richard YANG - Mar 06, 2025, 5:06 PM CST





<u>Download</u>

Screenshot_2025-03-06_at_5.05.12_PM.png (916 kB)



Richard YANG - Mar 13, 2025, 7:52 PM CDT

Title: CMRR & SNR calculations

Date: 3/13

Content by: Richard

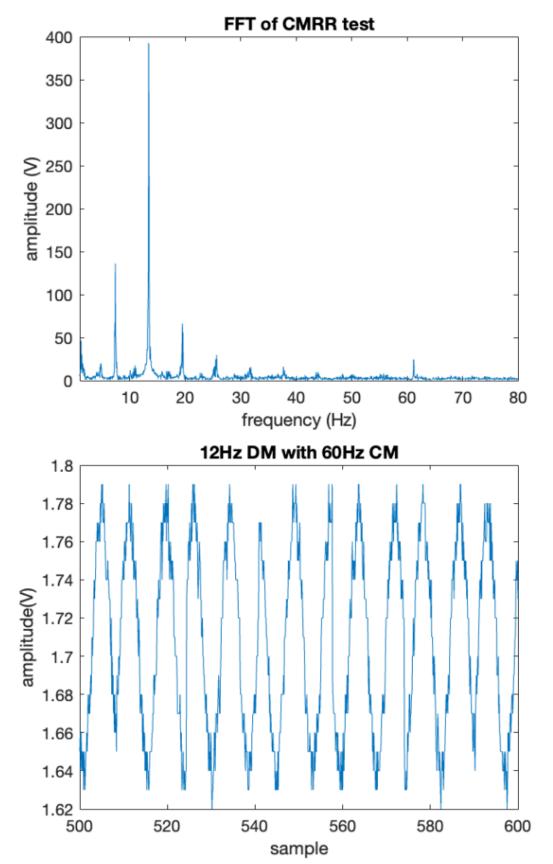
Present: Richard, Ellie

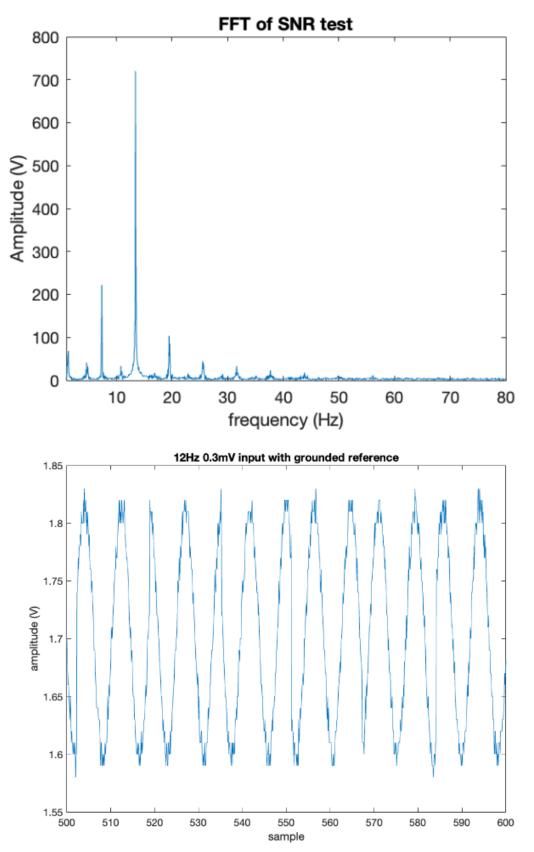
Goals: calculate relevant performance parameters

Content:

CMRR test is conducted with V_in at 120mV*sin(2pi*12)+20mV*sin(2pi*60) and v_ref at 20mVs*sin(2pi*60). The CMRR is found to be 2.65 V/V or 8.5 dB.

SNR test is conducted with V_in at 0.3mV*sin(2pi*12) and v_ref grounded. The SNR is found to be 3740 V/V or 71.5 dB.





Conclusions/action items:



Richard YANG - Apr 18, 2025, 11:11 AM CDT

Title: making visualization figures

Date: 4/18

Content by: Richard

Present: NA

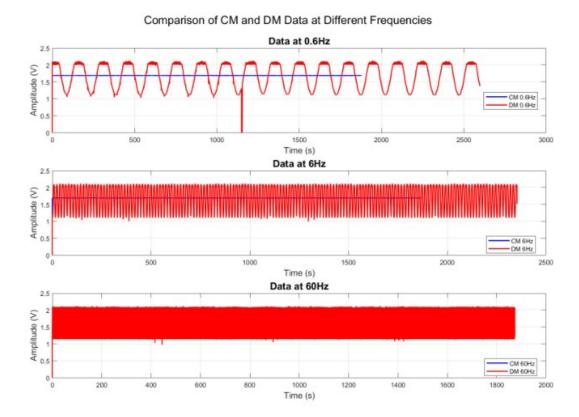
Goals: make figures for the poster presentation

Content:

Wrote Matlab code to visualize data. Written in a format that allows dynamic "plug-and-play" visualization.

We observe some clipping on the positive end. Upon investigation, this is due to the DC-DC convertor outputting only -1.3 V for Vss.

This problem occurs at the bandpass filter when the signal is inverted, so it shows up as clipping on the positive range when it is inverted again at the level shifter.



Conclusions/action items:

Calculate CMRR for each frequency. Fix the dc-dc convertor issue.

2025/2/25 - EEG Background info with Epilepsy

155 of 178

ELLIOTT HARRIS - Sep 13, 2024, 8:49 AM CDT

Title: EEG Background info

Date: 9/12/24

Content by: Elliott Harris

Present: N/A

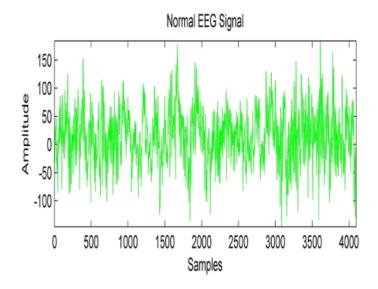
Goals: Understand how EEG detects Epilepsy and what technology exists.

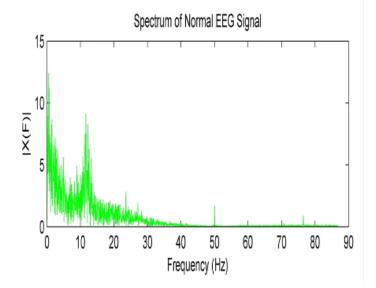
Content:

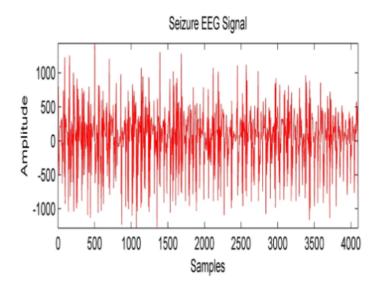
Electroencephalogram (EEG) is one of the most common methods used for seizure detection as it records the electrical activity of the brain. Symmetry and asymmetry of EEG signals can be used as indicators of epileptic seizures.

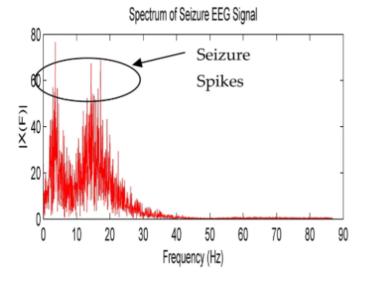
Normally, EEG signals are symmetrical in nature, with similar patterns on both sides of the brain. However, during a seizure, there may be a sudden increase in the electrical activity in one hemisphere of the brain, causing asymmetry in the EEG signal. In patients with epilepsy, interictal EEG may show asymmetric spikes or sharp waves, indicating the presence of epileptic activity. Therefore, the detection of symmetry/asymmetry in EEG signals can be used as a useful tool in the diagnosis and management of epilepsy.

The analysis and diagnosis of epileptic seizures are commonly done using EEG signals by medical practitioners. The interpretation of EEG signals by expert physicians and medical practitioners requires more effort and time. An automatic seizure detection system will help the practitioners to study and analyze the EEG signal with ease, reducing their effort and time significantly.









Sep 29, 2024, 9:41 AM CDT

Conclusions/action items:

Use this knowledge to make decisions on how we will create our design.

Comments

Amit Nimunkar

Please add some entries with regards to circuits for EEG acquisitions and processing.



2025/4/27-EEG Electrode Placement

ELLIOTT HARRIS - May 04, 2025, 8:01 PM CDT

Title: EEG Electrode Placement

Date: 4/27/25

Content by: Elliott Harris

Present: N/A

Goals: Research the reasoning behind the placement of electrodes so we can understand where to place them in our design.

https://naxonlabs.com/blog/understanding-strategic-placement-sensors-eeg-devices

Content:.

Typically uses a 10-20 system which is referring to the percentage of the surface area of the brain that is covered in between electrodes.

1. TP9 and TP10: Temporal Lobes

Location: Just behind the ears, covering the left and right temporal lobes.

Importance: The temporal lobes are vital for emotional processing, including the interpretation of emotional speech cues, recognition of facial expressions, and formation of emotional memories. Sensors TP9 and TP10 help capture brain responses to emotional stimuli, offering insights into how emotional content is processed, whether through auditory or visual cues.

2. AF7 and AF8: Prefrontal Cortex

Location: On the forehead, adjacent to the hairline, situated over the prefrontal cortex on both sides.

Importance: The prefrontal cortex is key to regulating and controlling emotions. The data from sensors AF7 and AF8 shed light on emotional regulation processes, revealing the mechanisms of emotion expression and management.

AF (Anterior Frontal): Situated between the prefrontal (Fp) and frontal (F) regions, providing insights into prefrontal cortex activities that underpin decision-making, social behavior, and personality.

FC (Fronto-Central): Located between the frontal (F) and central (C) areas, crucial for motor function control and higher cognitive processes.

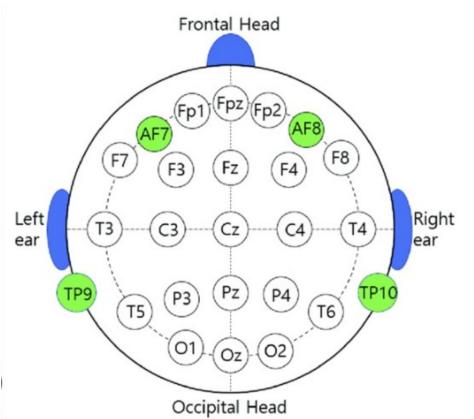
FT (Fronto-Temporal): Bridges the frontal (F) and temporal (T) regions, key for understanding the integration of auditory information and language processing.

CP (Centro-Parietal): Nestled between central (C) and parietal (P) lobes, significant for sensory integration and spatial orientation.

TP (Temporo-Parietal): Between temporal (T) and parietal (P) lobes, important for auditory perception, language comprehension, and social cognition.

PO (Parieto-Occipital): Lies between parietal (P) and occipital (O) regions, essential for visual processing integration.

Additionally, the MCN revises the labeling of some electrodes to align with this expanded framework, renaming T3 to T7, T4 to T8, T5 to P7, and T6 to P8, thereby enhancing the specificity of temporal and parietal monitoring.



Conclusions/action items:

Create design based off this information.

2025/4/28-EEG Placement for Epilepsy Detection

ELLIOTT HARRIS - May 04, 2025, 8:01 PM CDT

Title: Epilepsy Detection Electrode Placement

Date: 4/28/25

Content by: Elliott Harris

Present: N/A

Goals: Determine which locations on the electrode map are important to use.

https://www.ncbi.nlm.nih.gov/pmc/articles/PMC10154941/

Content:

- Channel selection involves applying a computational or statistical methodology such as machine learning to extract the channels with the most importance at any given moment. If machine learning techniques are used, then sensitivity and specificity scores are applied to the result, indicating whether the model successfully extracted the most important channels.
- The important channels can be selected across a group of patients, or they can be patient specific, inferring unique channels for individual patients depending on their epilepsy type and onset zone.
- The 'Insight' device by EMOTIV (EMOTIV) offers five channels, while the Neurotrail by Neuro-Pro AG starts at eight electrodes and can be reduced to one; both utilize dry electrodes. The Advanced Brain Monitoring device (Advanced Brain Monitoring Inc.) also offers multi-modal signal fusion, using three frontopolar channels to record EEG, electrooculography and electromyography signals. Ceribell Inc. offers an eight-channel seizure monitoring device with an inbuilt seizure alert system, making it advantageous for low-resource or intensive care settings where experienced clinicians may not be available.
- the requirement to place it on a hairless skin patch (such as behind the ear) may be an advantage of the device given the growing interest in 'behind-the-ear' or 'in-ear' EEG.

Conclusions/action items:

Create design based off this data.



ELLIOTT HARRIS - Jan 31, 2025, 1:07 PM CST

Title: New Ear Clip Design

Date: 1/30/25

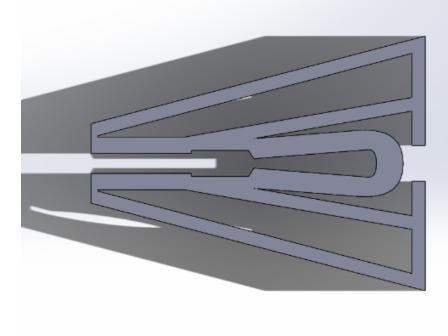
Content by: Elliott Harris

Present: N/A

Goals: Create a new mechanism that prevents the ear clip from failing after a couple of uses.

Content:

Added stopping mechanism that doesn't allow the user to overexert the mechanism that caused failure previously.



Conclusions/action items:

Have team member 3D print this design and then start to attach electrodes based off of how well it works.

2025/2/21 - Waissman Center EEG

ELLIOTT HARRIS - Feb 25, 2025, 10:44 AM CST

Title: Waissman Center EEG

Date: 2/21/25

Content by: Elliott Harris

Present: N/A

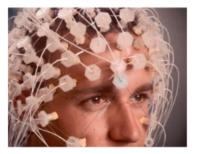
Goals: Create questions for the Waissman Center to clarify the use of head cap and ear clip.

Content:



The Waisman Brain Imaging Core houses a Magstim EGI Net Amps 400 Electroencephalogram (EEG) recording system for the acquisition of high-density EEG and ERP data. This system offers a high impedance amplifier that can be suitable in multiple environments and the Geodesic Sensor Net allows sensors to be applied simultaneously and easy to use across various populations, including infants, toddlers and children. The 128-channel system provides high spatial and temporal resolution with whole head coverage, making it ideal for studies to measure brain activity changes in complex neurodevelopmental disorders and neurological diseases.

Data collection is achieved using EGI's Net Station 5 software package which is installed on a iMac Desktop computer in the EEG control room. The Net Station 5 software package is engineered for easy acquisition and allows review of both standard EEG montages (such as 10–20 and 10–10), or High-Density EEG with up to 256 channels in a networked environment. Net Station 5 also provides synchronized chart plots, topo plots, topo maps and interactive 3D scalp voltage depiction.



The system uses Geodesic Sensor Nets that come in a range of different sizes (from 28 cm for preterm infants to 64 cm for adults) and allows us the flexibility to test subjects with different head sizes. These nets have been designed to be easy to use, comfortable and can produce high-quality and high-

resolution data. Individual studies and/or labs will be responsible for purchasing and maintaining (e.g. cleaning) their own Geodesic Sensor Nets.

For more information regarding the WBIC EEG system please reach out to Michael Anderle.

- Is a head cap necessary?
- What aspects of the head cap/net are important for an EEG test? (Secure connection, comfort, etc.)
- Does your system include an ear clip electrode? What is the importance of grounding at the ear?
- Can we ground the system somewhere else on the body?
- How important are the locations of the electrodes on the head?
- What are the downsides of having incorrect electrode placements?
- If we were to compare our system with their system, how would we go about doing this? Is this possible?

Conclusions/action items:

Hopefully get a response next week and set up a meeting with the individual there.



ELLIOTT HARRIS - Feb 28, 2025, 11:24 AM CST

Title: Newest Ear Clip Design

Date: 2/26/25

Content by: Elliott Harris

Present: N/A

Goals: Create new ear clip to print and fabricate with electrode

Content:

- Edited ear clip to have stopping mechanism to prevent over exertion
- create more space for placement of electrode onto the ear clip
- See attachments

Conclusions/action items:

Print the following ear clip.

ELLIOTT HARRIS - Feb 26, 2025, 1:35 PM CST



Download

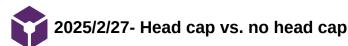
NewestEarClip.SLDPRT (189 kB)

ELLIOTT HARRIS - Apr 23, 2025, 10:08 PM CDT



Download

NewestEarClip.STL (18.5 kB)



ELLIOTT HARRIS - Feb 28, 2025, 11:43 AM CST

Title: Head cap vs. no head cap

Date: 2/27/25

Content by: Elliott Harris

Present: N/A

Goals: Research why a head cap is used and what the advantages and disadvantages are of both.

Content:

https://brainshapeva.com/to-cap-or-not-to-cap/

This is an anecdote from an EEG expert. She conducts EEG tests and originally used EEG head caps but then switched to the no head cap system

She uses a gel that helps adhere the electrode to the scalp and conduct the tests

She noticed her patients were experiencing pain while using the head caps and this is why she switched

Pros of no head cap:

- no pain
- · don't have to deal with placing gel underneath the head cap
- · easy to make adjustments to electrodes to get better signal

Cons of no head cap:

- You must know the 10-20 system and still isn't perfect
- · takes longer to set up and conduct a test
- much more difficult to keep consistent

Conclusions/action items:

Testing both methods would be possible and something that we could do in order to determine which system would be most effective.



ELLIOTT HARRIS - Apr 17, 2025, 11:51 PM CDT

Title: Meeting to Discuss Further Testing

Date: 3/14/25

Content by: Elliott Harris

Present: Mark

Goals: Get an idea of further testing that can be conducted for the hardware.

Content:

- Came up with durability testing
- Testing the effectiveness of the head cap vs. the Weismann centers set up
- Creation of the package for our design
- Testing the package security and durability

Conclusions/action items:

Conduct the previous listed tests.



ELLIOTT HARRIS - Apr 17, 2025, 11:53 PM CDT

Title: Pre outreach meeting

Date: 4/5/25

Content by: Elliott Harris

Present: All

Goals: Create a presentation and plan for our outreach activities.

Content:

We met as a team and created our presentation for the outreach activities. We went over what each of us will do for the outreach activity. Since I was not going to be there I reached out to Dr. P to see what she would have me do instead.

Conclusions/action items:

Conduct the outreach activity that week.



ELLIOTT HARRIS - Apr 17, 2025, 11:55 PM CDT

Title: BME Outreach Activity Make Up

Date: 4/6/25

Content by: Elliott Harris

Present: Professor Puccinelli

Goals: Find an alternative assignment for me to complete and get credit for the outreach activities.

Content:

I met with Professor P and she led me to the supply cabinet where she had a lot of materials to be organized and placed into the closet correctly. I then went to the closet and organized the materials to the best of my ability and threw away any unusable material and things they weren't using.

Conclusions/action items:

Complete the activity.



ELLIOTT HARRIS - Apr 18, 2025, 7:44 AM CDT

Title: Case Durability Testing Plan

Date: 4/15/25

Content by: Elliott Harris

Present: Mark

Goals: Create a plan for the case durability testing and what will be completed for this test.

Content:

Objective:

evaluate the durability of the EEG cap case prototype from common wear and tear use like accidental drops.

Scope

This will be done with a empty circuit board since we do not have extra components that can be damaged, further work can be considered with a full circuit prototype on board to evaluate if it can still function. For now it will look for cosmetic damage, damage to the circuitboard and how well the board stays screwed in.

Test Equipment

Calipers, phone camera for video and photo analysis, 1 3d printed prototype made from PLA for damage testing and 1 for an undamaged control, hard floor like concrete, wood, stone etc.

Drop heights

0.75 m, 1m, 1.2m or as necessary to see damage

Drop orientations (starting in this position):

Flat on base

Flat on top

Flat on front face

Flat on back face

Flat on left side

Flat on right side

One top front edge

One corner

Test procedure:

starting at 0.75m, randomly select an orientation and drop while recording with a camera. Take photos of any changes in damage, record if the damage is: cosmetic, functional and if the damage is: minor (can still be used for normal function) moderate (still works but is badly cosmetically damaged) or severe (cannot continue under normal function).

Acceptance criteria

The product is acceptable if it makes it through all orientations at all 3 heights with only receiving minor or moderate cosmetic damage, not severe damage.

Conclusions/action items:

Complete the test this weekend.



Mark RICE - Apr 18, 2025, 12:14 PM CDT

Title: Weismann Center Contact
Date: 4/15/25
Content by: Elliott Harris
Present: N/A
Goals: Get information regarding our project and make appointment to meet at the Weismann Center to compare systems.
Content:
Reached out to Weismann Center for information regarding EEG hardware. Received the following response:

Sorry for the delay. I'm wondering if you'd want to come take a look at our EEG system? Would you be available sometime next week?

To try to answer a few of your questions, but will preface this that I'm not an EEG expert but am learning more about EEG as we are using it for a large, consortium study.

1) You definitely want/need to have a secure connection that is close to the scalp as possible. This will help improve the SNR and allow you to collect the best data. That said, comfort for the participants are also critical as they may complain about the net and not want to continue. I study infants and children, and if the net is uncomfortable, then they will likely cry or try to remove the net themselves.

2) I don't think our system has an ear clip electrode, and can't really say what the importance to grounding to the ear is.

3) Location of the electrodes is important for knowing what areas of the brain you are receiving signal from. So downsides would be not knowing where in the brain the signals are being generated from.

4) I think to compare your system to ours, you would need to think about the type of tests you would need to run. You would probably want to run tests/acquire data from the same participants on both systems.

Best,

Hi Elliot,

Doug

Conclusions/action items:

Utilize this information in our design and ask the person to meet regarding their system.





ELLIOTT HARRIS - Apr 17, 2025, 11:44 PM CDT

Title:

Date:

Content by:

Present:

Goals:

Content:

Conclusions/action items:



Title: Ear Clip Force Testing

Date: 3/6/25

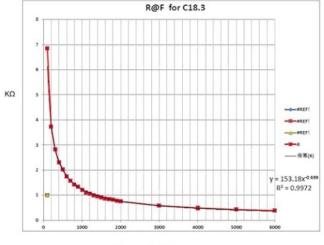
Content by: Elliott Harris

Present: N/A

Goals: Test the amount of pressure produced by the ear clip at different ear lobe thicknesses.

Content:

The figure below shows a curve of resistance as a function of pressure under specific test conditions



Pressure (mmHg)

Y = $153.18 \times (-0.699)$ where Y is resistance in KOhms and X is pressure in mmHg

Materials Needed:

- 1. Ear clip
- 2. Pressure-sensitive resistor (FSR)
- 3. Multimeter
- 4. Notebook with removable pages
- 5. Calibration curve equation for the pressure-sensitive resistor
- 6. Ruler or caliper (to measure thickness)
- 7. 7 different thicknesses of paper stacks: 4mm, 5mm, 6mm, 7mm, 8mm, 9mm, 10mm

Step-by-Step Procedure:

Preparation:

- 1. Prepare the Notebook:
 - Remove pages from the notebook to create stacks of paper with the following thicknesses: 4mm, 5mm, 6mm, 7mm, 8mm, 9mm, and 10mm.
 - Use a ruler or caliper to measure and confirm the thickness of each stack.

170 of 178

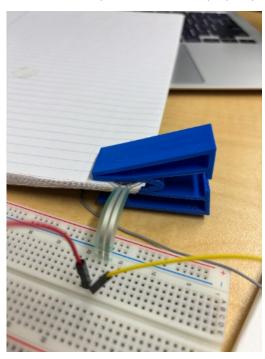
Elliott Harris/Testing/2025/3/6- Force Testing





1. Set Up the Pressure-Sensitive Resistor:

• Place the pressure-sensitive resistor (FSR) on top of the paper stack. Ensure it is positioned flat and stable.



1. Connect the Multimeter:

• Attach the multimeter probes to the leads of the pressure-sensitive resistor. Set the multimeter to measure resistance (Kohms, KΩ).

Testing Procedure:

4. Test for Each Thickness:

• Begin with the 4mm stack. Place the ear clip onto the pressure-sensitive resistor, ensuring it is clipped securely and evenly.

5. Record Resistance:

• Read the resistance value displayed on the multimeter. Record this value in a data table.

6. Calculate Pressure:

• Use the calibration curve equation for the pressure-sensitive resistor to convert the recorded resistance value into pressure (e.g., Pascals or mmHg).

7. Repeat for All Thicknesses:

• Repeat steps 4-6 for each of the remaining thicknesses (5mm, 6mm, 7mm, 8mm, 9mm, and 10mm).

8. Ensure Consistency:

• For each thickness, ensure the ear clip is applied with the same force and positioning to maintain consistency across tests.

Ear Clip Pressure Test Data Table

Thickness (mm)	Trial 1 Resistance (KΩ)	Trial 1 Pressure (mmHg)	Trial 2 Resistance (KΩ)	Trial 2 Pressure (mmHg)	Trial 3 Resistance (KΩ)	Trial 3 Pressure (mmHg)	Average Pressure (mmHg)
4	205.5	0.62	196.1	0.67	238.4	0.53	0.61
5	172.4	0.83	183.2	0.77	150.5	1.02	0.87
6	98.6	2.02	110.4	1.73	95.6	2.12	1.96
7	68.6	3.43	54.6	4.81	58.0	4.42	4.22
8	39.7	7.82	45.8	6.42	42.9	7.05	7.10
9	35.9	8.12	35.4	8.26	30.3	10.45	8.94
10	20.7	17.82	23.4	14.92	27.8	11.89	14.88

https://pubmed.ncbi.nlm.nih.gov/23134900/

Probes exerted an average of 0.24 lb (SD 0.6) of force over an area of 0.3 square inches, equal to an average of 20.7 mm Hg (SD 0.6) pressure on tissue. In ICU patients there have been pressure ulcers that have formed at this pressure. So any values of 20 mmHg - 30mmHg and beyond can cause pain and discomfort.

 $https://musemond.com/pages/size-guide?srsltid=AfmBOoq4nGltfesJHJK-bkltSGY28OuRoFW24AS56WK56qH-xSLJx_9fmtestreproductions and the second seco$

Lobe/Second Lobe: Standard: 6mm | Thin Ear: 5mm | Thick Ear: 7-8mm

Conclusions/action items:

Pressure was very low at low thicknesses. Would like to change design to get a higher pressure at those lower thicknesses.



ELLIOTT HARRIS - Apr 04, 2025, 11:04 AM CDT

Title: Durability Testing

Date: 4/2/25

Content by: Elliott Harris

Present: N/A

Goals: Conduct durability testing.

Content:

Step-by-Step Testing Procedure:

1. Pre-Test Setup

- Visually inspect each ear clip for initial defects (warping, layer inconsistencies, etc.).
- Measure and record the original dimensions (e.g., clip opening distance).

2. Testing Setup

- Testing manually:
 - Use a consistent hand compression method (same force each time).
 - Have a counter to track compressions.

3. Testing Execution

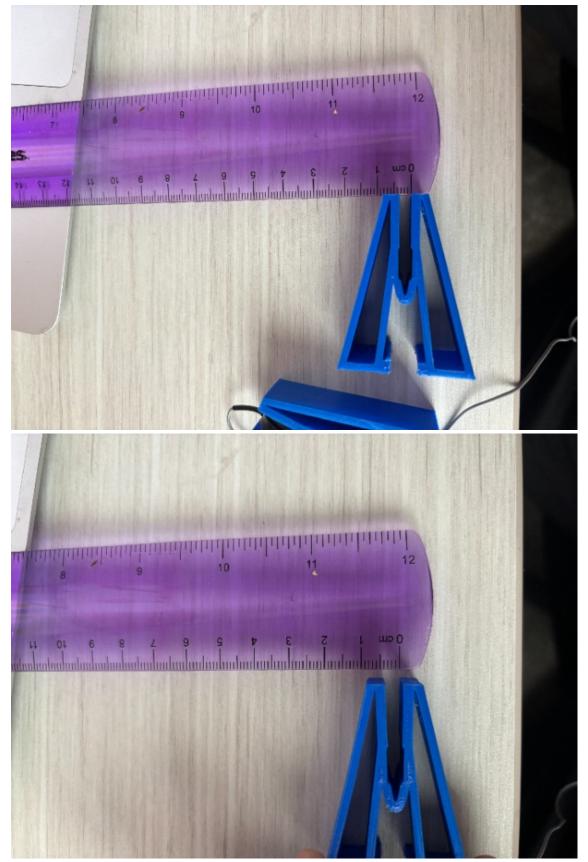
- For each design (A, B, C), perform the following:
 - 1. Mount the ear clip securely in the testing fixture.
 - 2. Begin compressing and releasing the clip repeatedly.
 - 3. After every 10 cycles, or if needed, pause and inspect for:
 - Cracks or visible damage
 - Permanent deformation (failure to return to original shape)
 - Loss of clamping force
 - 4. Continue until the clip fails (defined as permanent deformation, breakage, or inability to function).
 - 5. Record the total number of cycles at failure.

4. Post-Test Analysis

- · Compare the failure points of all three designs.
- Note the failure mode (hinge breakage, arm fracture, fatigue deformation).
- Document any observations

Data Collection Table

Test #	Design	Initial Opening Dimension (mm)	Cycles Completed	Failure Mode	Notes
1	Design A	3	56	Fatigue deformation	Opening changed from 3mm to 4mm
2	Design B	3	14	hinge breakage	Failed in the opening mechanism
3	Design C	0	200	N/A	Did not fail



Elliott Harris/Testing/2025/4/2 - Durability Testing



Conclusions/action items:

Utilize this data as evidence of meeting design specifications.



John Puccinelli - Sep 05, 2016, 1:18 PM CDT

Use this as a guide for every entry

- Every text entry of your notebook should have the **bold titles** below.
- Every page/entry should be **named starting with the date** of the entry's first creation/activity. subsequent material from future dates can be added later.

You can create a copy of the blank template by first opening the desired folder, clicking on "New", selecting "Copy Existing Page...", and then select "2014/11/03-Template")

Title: Descriptive title (i.e. Client Meeting)

Date: 9/5/2016

Content by: The one person who wrote the content

Present: Names of those present if more than just you (not necessary for individual work)

Goals: Establish clear goals for all text entries (meetings, individual work, etc.).

Content:

Contains clear and organized notes (also includes any references used)

Conclusions/action items:

Recap only the most significant findings and/or action items resulting from the entry.



Title:			
Date:			
Content by:			
Present:			
Goals:			
Content:			

Conclusions/action items: