Final Deliverables

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Section 302

Affordable Diagnostic EEG System for Viral-induced Epilepsy

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Abstract

Epilepsy is a prevalent neurological disorder affecting 50 million people worldwide. 80% of epilepsy patients live in low- and middle-income countries where expensive EEG systems are not accessible. This project aims to fill the critical need for accessible diagnostic devices for epilepsy by developing a cost-effective EEG system. The team developed a TPU 3D-printed head cap, ear clips to house reference and driven right leg electrodes, and the analog front end on a printed circuit board. The head cap shows a 5.8% to 7.3% mean absolute error in landmark alignment. The ear clips were found to be comfortable among participants, with an initial average Borg score of 7.25 and a 10-minute score of 9.75. The analog front end has not been thoroughly tested, but preliminary results show frequency response as designed (0.1 Hz to 200 Hz) and promising amplification fidelity.

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Introduction

It is estimated that 1 in 26 Americans develops Epilepsy at some point in their lifetime. Epilepsy is a neurological disorder that causes sporadic seizures affecting 50 million people worldwide[1]. Various treatments exist for Epilepsy, such as anti-seizure medications (AEDs), ketogenic diets, seizure-preventing devices, and even surgery [2]. However, diagnosis of the sub-type of Epilepsy is required before a treatment plan can be devised. The primary way to detect Epilepsy without observing recurring seizures is through an electroencephalogram (EEG) [3]. The EEG system is placed on the patient's scalp and is used to detect the electrical impulses in the human brain. Currently, EEG devices are expensive and difficult to obtain. Medical-grade EEG systems cost tens of thousands of dollars, and open-source projects are still prohibitively expensive. OpenBCI, a partially open-source project known for its brain-computer interface devices, offers an eight-channel biosensing board, EEG cap, and electrodes for $2,578 [4]. Although this device may be effective, areas without the necessary resources could not afford a stock of these devices to detect and diagnose epilepsy. 80% of epilepsy patients live in low- and middle-income countries, the majority of whom have access to treatment but not diagnostic equipment [5]. This project aims to create a reliable, accurate, and inexpensive EEG device. The product must receive, process, and display signals from ten channels in a format that a medical professional can easily interpret.

Background

Epilepsy is a brain disorder characterized by abnormal neuron activity, leading to misfires in the brain and resulting in seizures. Two or more of these seizures, with an unknown cause, is what is called Epilepsy. Anyone at any age can develop Epilepsy. However, it is most common in early childhood or old age [1]. Conventionally, EEG uses scalp electrodes that record a variety of active neuronal potential fluctuations. The potentials are aggregations of neuronal action potentials [6]. These recordings usually range from 0.5 to 100 Hz and their amplitudes ranges from 5 μV to 300 μV [6]. An example EEG of absence seizure is shown in Figure 1 and is characterized by a behavioral arresting with concurrent 3-Hz wave discharges [7]. EEG can detect miscommunications between neurons. These channels that detect those miscommunications will tell the physician that the patient may have epilepsy. Using more channels across different brain regions can give a higher chance of detecting these disruptions in brain activity. One study found that Epilepsy affects the hippocampus, amygdala, frontal cortex, temporal cortex, and olfactory cortex most often. However, disruptive activity can be detected across many brain regions [8]. This justifies the constraint of 10 channels rather than eight or fewer channels, giving a higher chance of detection.

Neurodiagnostic tests like EEG are challenging to perform in less fortunate areas. A study completed by the American Academy of Neurology says that in most low-income countries surveyed during the study, only the top 10% or 20% of the population could afford tests below catastrophic levels. In surveyed lower-middle-income countries, >40% of the population, on average, could not afford neurodiagnostic tests [3].

This is in stark contrast to high-income countries like the United States, and Western Pacific World Health Organization regions, where more than 70% of the total population can afford EEG tests [3]. Dr. Brandon Coventry, a postdoctoral fellow in the Department of Neurosurgery at the University of Wisconsin School of Medicine and Public Health, decided to create this project to find a way to solve this problem. For the device to be useful for less fortunate areas, Dr. Coventry aims to keep the production cost under 100 dollars. This device must also be compatible with various head shapes and sizes. The team found that the 50-64 cm circumference range would capture all regular occurring head sizes [9]. The device must remain in operation for 3-4 years without a dip in performance. The device must be able to be transported, stored, and implemented in a variety of temperatures depending on the environment. Please see Appendix A for the team's complete product design specifications for this product.

This project also includes the processing of low-amplitude signals from the brain. This consists of filtering and amplifying the signal. The design must be cost-effective and easy to fabricate. Filtering 60 Hz powerline noise is vital in any environment where capacitive coupling from the powerline and other electrical interferences exist. One commonly used filtering technique is a bandpass filter, which uses a circuit of varying electrical components to achieve a calculated sampling frequency. Instrumentation amplifiers are critical elements extensively used for input buffering and high voltage gain [10].

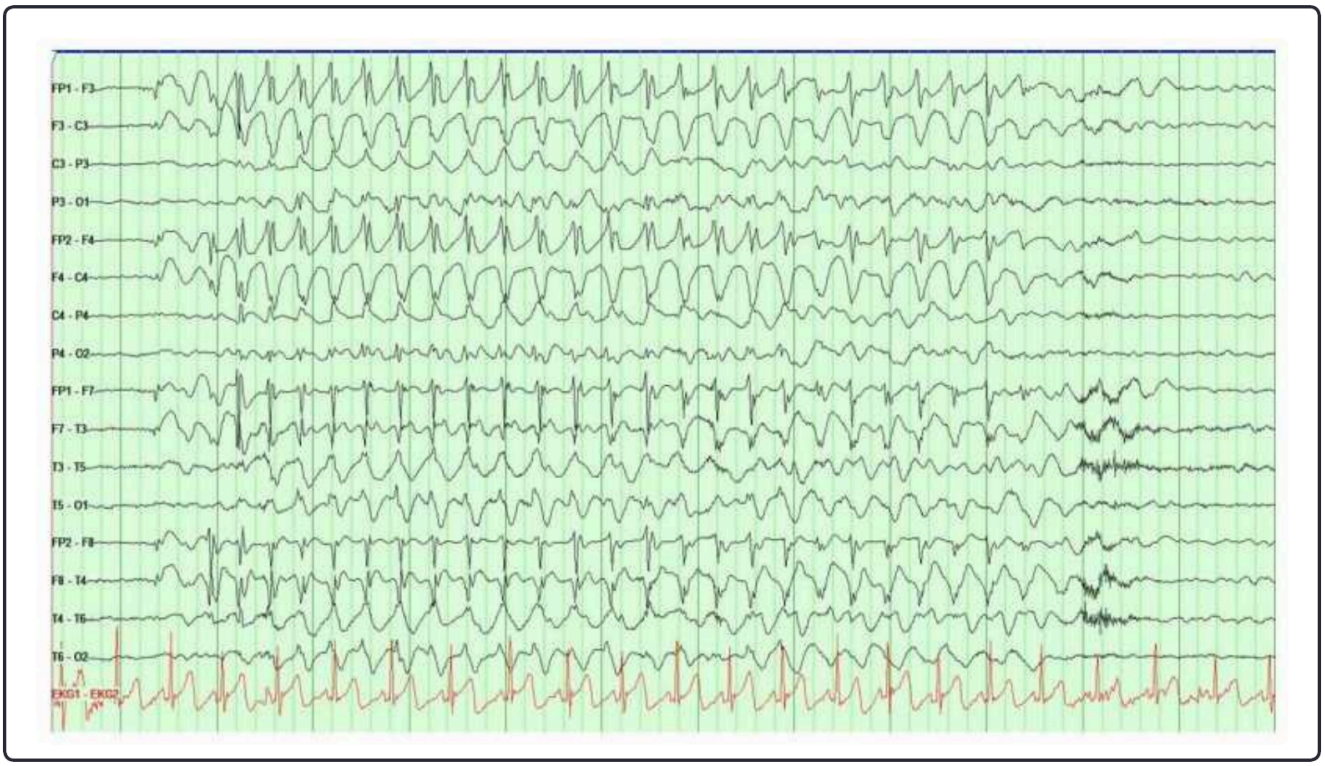


Figure 1: Example EEG of Absence Seizures [7]

Preliminary Designs

The full system includes a head cap to hold electrodes in place in the standard 10-20-20 layout, electrodes to acquire EEG signal, circuitry to filter and amplify the signal, an embedded system to read output from the circuitry, control parts of the circuit and output to an external PC, and finally, a GUI for reading and saving the acquired EEG signals from each channel on an external PC.

Head Cap

To acquire an accurate EEG signal, electrodes must be secured on the head in standardized placements, usually achieved through a head cap. The team explored four designs: store-bought head cap, DIY head cap, naked electrode, and 3D-printed head cap.

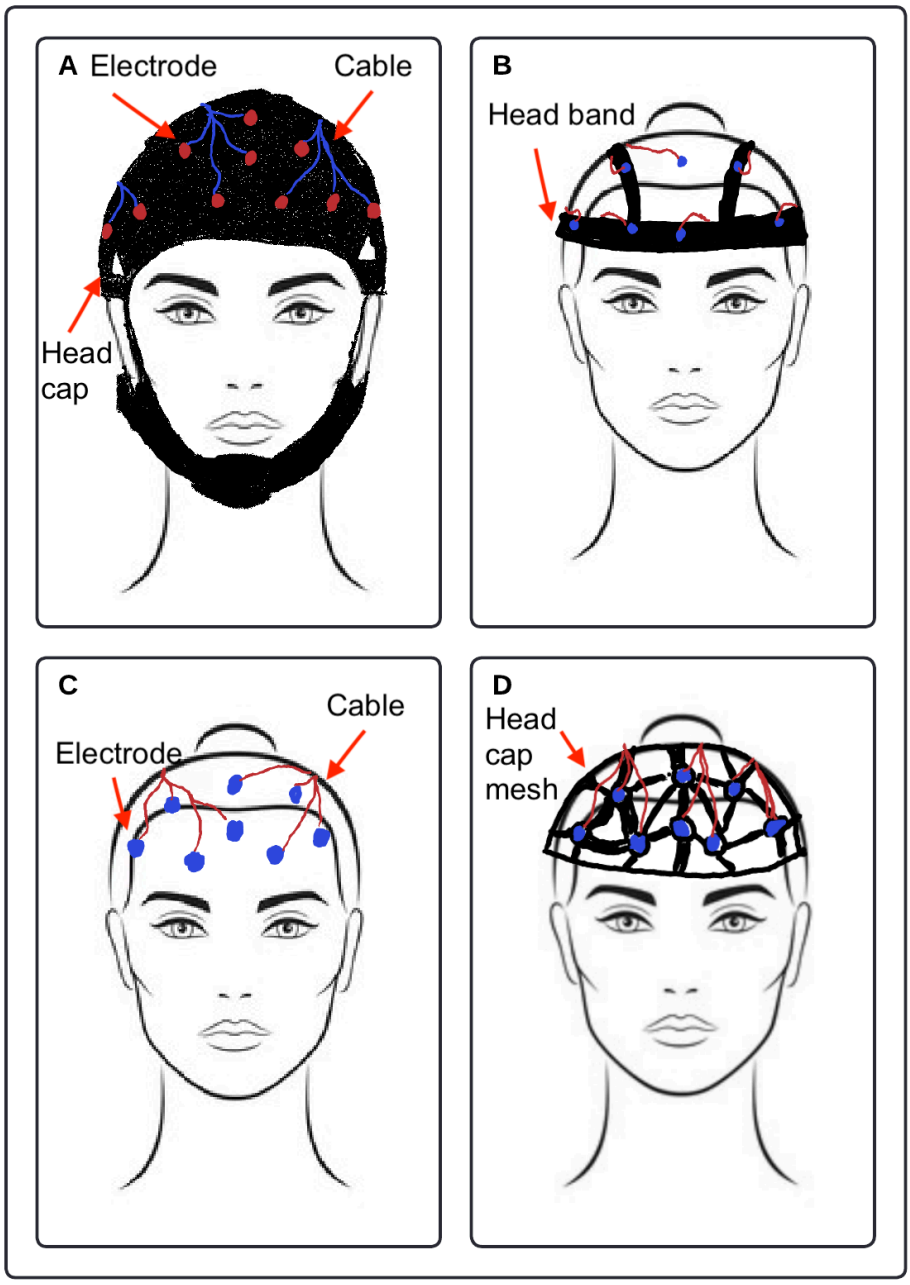


Figure 2: Preliminary Head Cap Designs. A. Store Bought Head Cap Concept Drawing where a headcap is worn that electrodes can be attached to and cables are managed externally. **B.** DIY Head Cap Concept Drawing where commonly used elastic materials are used to hold electrodes in place. **C.** Naked Electrodes Head Cap Concept Drawing where there is no external cap to hold electrodes on. **D.** 3D Printed Head Cap Concept Drawing where a 3D printed mesh is used to hold electrodes in place.

Store-bought Head Cap

Purchasing an already existing product gives the benefit of a tested market product that provides a reproducible reading each time. However, for an open-source project, a 3rd party head cap design is subject to potential hurdles such as price changes and supply chain availability in the given region.

Figure 2A shows a representative concept drawing of many available EEG cap designs similar to the OpenBCI Head Cap [11]. Commercially available EEG head caps like this may be at various prices. On the higher end, the OpenBCI Head Cap [11] costs around $500, while more cost-effective ones, like the Contec Head Cap [9], may cost only $16.

DIY Head Cap

To keep costs as low as possible, a “do it yourself” or DIY design was considered, and a set of measurements would be provided to modify common existing objects such as winter hats or baseball caps. This design, represented by Figure 2B, has limitations of repeatability. Misunderstanding of instructions could lead to incorrect measurements and potentially incorrect diagnosis. Additionally, each head cap would be different, providing varying readings, making design verification difficult.

Naked Electrode

A design without a head cap minimizes associated costs: the electrodes are placed directly on the scalp (Figure 2C). However, ensuring correct electrode placement and stability is a significant hurdle. All anatomical landmarks must be correctly manually identified, and electrodes must be consistently placed between tests.

3D-printed Head Cap

The final proposed design is a 3D printed head cap building off an existing pipeline that takes a computed tomography scan and provides a 3D printable design with the standard 10-20 placement [12] (Figure 2D). This design uses a mesh of flexible filament that helps to reliably find landmarks and gives open space for hair to be adjusted during electrode placement. Each cap uses about 20 grams of filament with support material excluded. It has been proven to work with thermoplastic polyurethane (TPU) [12], which has a Shore Hardness scale between 60A-77D and an approximate cost per gram of filament between $0.03-$0.08. This proposed design would consider alternative flexible filaments that cost less and attempt to build upon the design to minimize extra material used for supports.

Circuits

In addition to selecting a head cap, a circuit is required to accurately acquire the brain's signals. The circuit must include components to filter the signal and sample the waves at a rate of 1kHz. Two proposed circuits met the criteria.

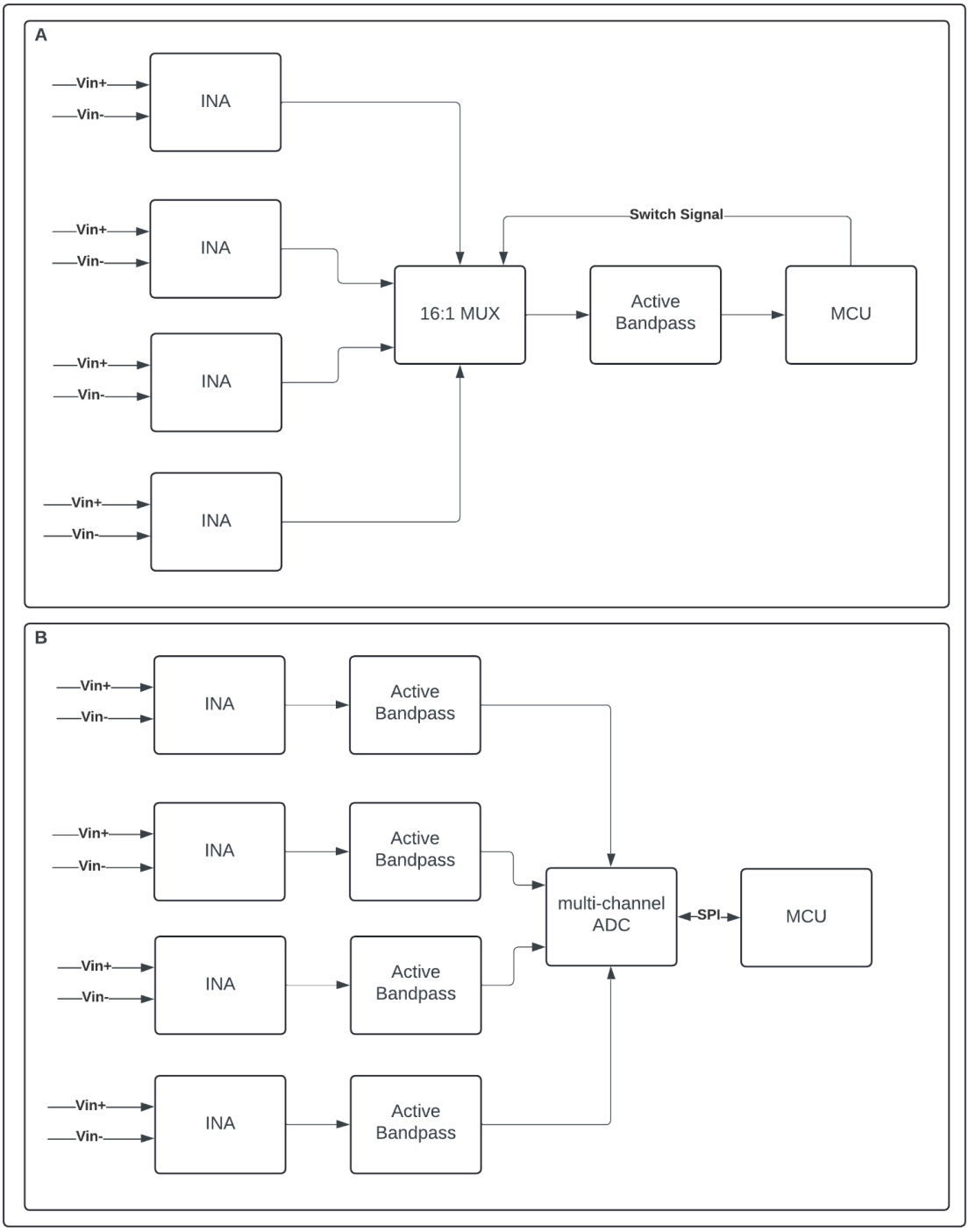


Figure 3: Preliminary Design of the Analog Front End. A. Circuit design with a single digital signal and multiplexer. **B.** Multi-channel ADC Circuit Connected to Front End

Single-channel Analog-to Digital Converter + Multiplexer

The first proposed circuit consisted of a single instrumentation amplifier (INA) connected to each electrode, which is then fed into a multiplexer (MUX) (Figure 3A). It cycles through each signal, sending one at a time through to the microcontroller (MCU). There is an additional set of circuitry to further ready the signal

for acquisition; all collected signals go through a single set of circuitry due to the multiplexer. The signal is then collected from the Analog-to-Digital Converter (ADC) onboard the MCU.

Multi-Channel Analog-to-Digital Converter

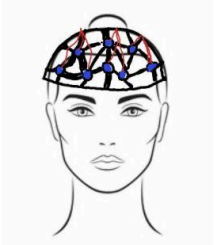
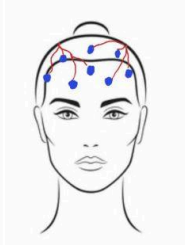
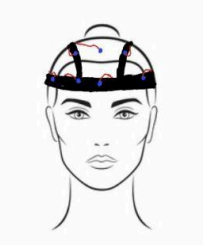
The second proposed circuit involves processing each signal through their dedicated instrumentation amplifiers and additional front-end circuitry (Figure 3B). A multi-channel ADC then collects these signals. It connects to the microcontroller via serial communication, which can then process and display every signal. This process involves ten bandpass filters and ten level shifters (among other signal processing units) for each electrode, unlike the one detailed previously.

Preliminary Design Evaluation

Proposed Final Head Cap Design

The following design matrix was proposed to evaluate the effectiveness of the proposed head cap designs. Each design was rated on a scale between 0 and the weight of that category, where the maximum possible score for each design is 100. Each design was rated based on the overall cost of that solution, the safety for the person wearing the head cap, meaning electrodes were secure, how accurately each electrode would be placed on the standard 10-20 electrode markers, how repeatable the design is, meaning each time it was created, it would have the identical dimensions and each time it was used given the same inputs it would provide the same outputs, ease of use for the person administering the test, how comfortable the design would be on the person receiving the test and finally how easy each would be to fabricate including either production, assembly or purchasing.

Table 1: Head Cap Design Matrix

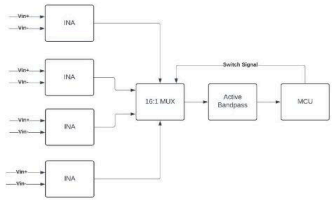
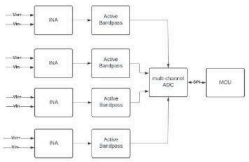
					
	Store Bought	**3D Printed**	**No Head Cap**	**DIY**	**Weights**
Cost	0	16	20	16	20
Safety	15	12	9	9	15
Accuracy	14	11	3	6	14
Repeatability	11	14	3	6	14
Ease of Use	13	10	5	5	13
Durability	12	7	10	5	12
Comfort	7	6	6	4	7
Ease of Fabrication	5	2	5	3	5
Total	**77**	**78**	**60**	**53**	100

While the Store Bought design did have the highest score in the majority of categories, due to the highest quality designs having a cost higher than the entire cost of this product, the 3D printed design was chosen to continue as the proposed final design. For more details, see Appendix B.

Proposed Final Circuit Design

A design matrix was also proposed to evaluate the various circuit designs. Similar to the head caps, a rating scale was created where a maximum of 100 could be achieved for each design. The designs were compared against one another in several categories, with the most weight being awarded to cost, as well as how accurate the signal collection would be. Other categories of rating included how easy it would be to fabricate the design, how difficult it would be to code the analysis and display of the signals, and how available the components would be for purchases; this includes how easy it is to swap one component for another readily available on the market. These categories were placed in the design matrix, as seen below in Table 2.

Table 2: Circuit Design Matrix

			
	Single-channel ADC + MUX	**Multi-channel ADC**	**Weights**
Cost	26	16	26
Accuracy	16	21	26
Ease of fabrication	20	15	25
Firmware Complexity	5	3	5
Components Availability	14	10	17
Sum	**81**	**65**	100

From the design matrix, it can be seen that the single channel ADC + MUX is the clear winner. The cost of this design is much less due to the decreased number of op-amps and because the reduced circuitry wins in both fabrication ease and component availability. It is also easier to code as there is only one signal, allowing for easier processing. The only category it loses in is accuracy, as it has to switch between 10 different signals. However, by allowing time for the signal to stabilize, switching artifacts can be minimized, avoiding inaccurate readings. Thus, the single-channel ADC + MUX design has been selected. More information regarding the selection can be found in Appendix B.

Two configurations, parallel and series, of the proposed single-channel ADC + MUX design are developed in Altium Designer (Altium, San Diego). The goal of parallel configuration is to minimize switching artifacts, while the series configuration aims to reduce the number of components, consequently reducing cost. To compare the operational characteristics of the two configurations, five of each channel are printed on a PCB (PCBWay, Shenzhen, China) for testing. Each channel of the parallel configuration has a dedicated instrumentation amplifier, bandpass filter, level shifter, and variable gain amplifier (Figure 4A). All the channels then terminate at the MUX and are read directly by the ADC. Since each channel is independent from one another, they are ready to be sampled at any given time, and the only switching artifact produced is from the MUX itself. On the other hand, the series configuration only has a dedicated instrumentation amplifier and level

shifter for each channel (Figure 4B). Thus, on every switching event, the signal has to be stabilized not only across the MUX but also across the bandpass filter and the variable gain stage.

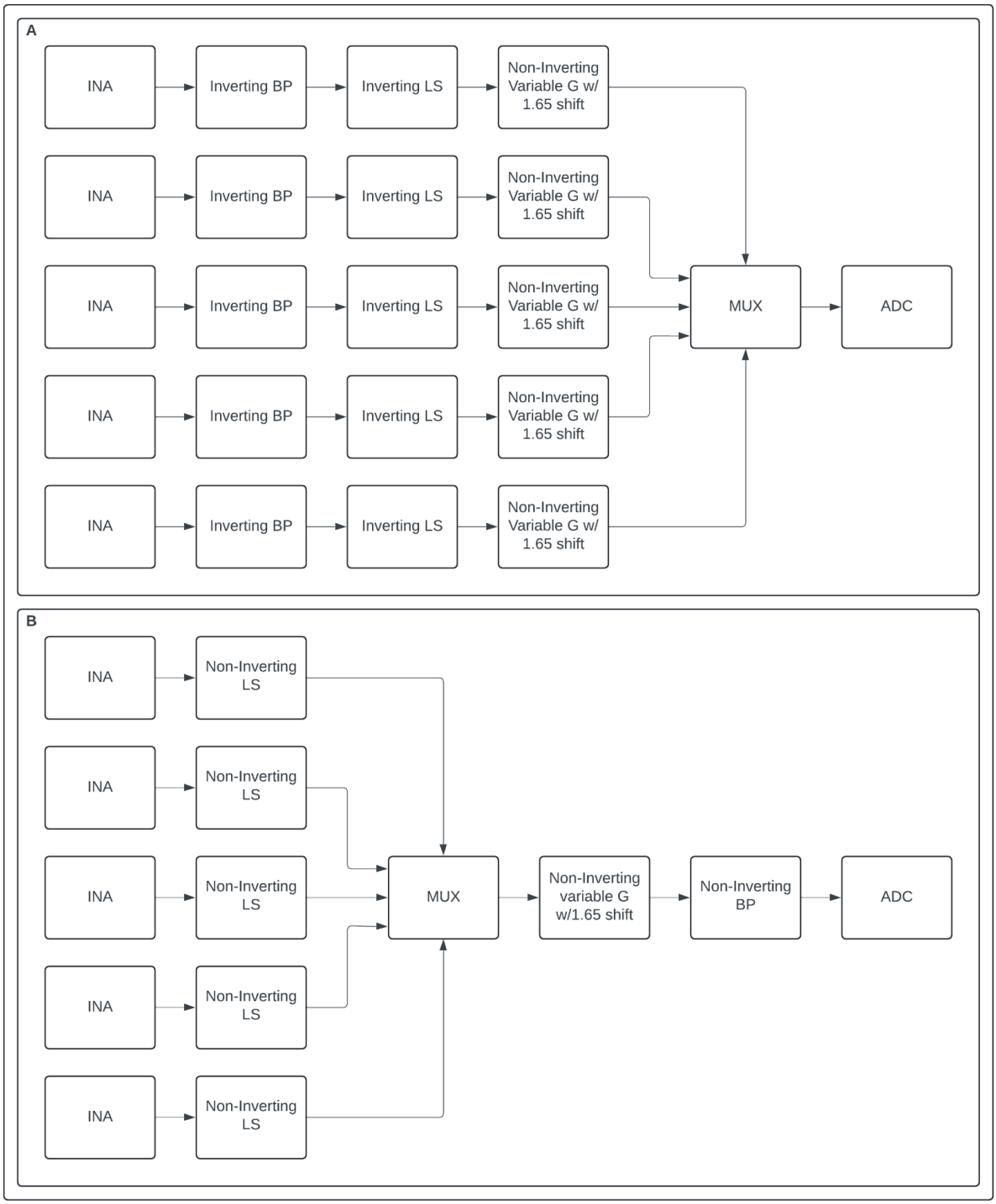


Figure 4: Block Diagrams of the Two Single-channel ADC Configurations. A. Block diagram of the parallel configuration. **B.** Block diagram of the series configuration.

The schematic diagram of a single channel of both configurations is shown in Figures 5A, 5B. Both bandpass filters are tuned to corner frequencies 0.1 Hz and 168 Hz with Equation 1. LT1920 is used as a

general-purpose instrumentation amplifier, and a fixed 10 kΩ resistor replaces the rheostat. For convenience, the MUX is modeled as a short.

$$f_c = \frac{1}{2\pi RC} \quad (1)$$

The gain of the INA is given by Equation 2 and the gain of the programmable amplifier is given by Equation 3. The gain for both level shifters is 0.5 V/V. For the parallel configuration, the bandpass filter has a gain of 26.9 V/V, while the series configuration has a gain of 27.9 V/V. Thus, the total gains of the parallel and series configurations are given by Equations 4 and 5, respectively. Importantly, for the series configuration, all the amplifiers have to be non-inverting since the level shifter must be placed first in front of the MUX. Therefore, if inverting amplifier topology is used, the positive DC shift induced by the level shifter will be come negative.

$$5 + \frac{80k\Omega}{R_G} \quad (2)$$

$$\frac{R_{Rheo}}{470} + 1 \quad (3)$$

$$2757 \times \left(\frac{R_{Rheo}}{470} + 1\right) \quad (4)$$

$$2857 \times \left(\frac{R_{Rheo}}{470} + 1\right) \quad (5)$$

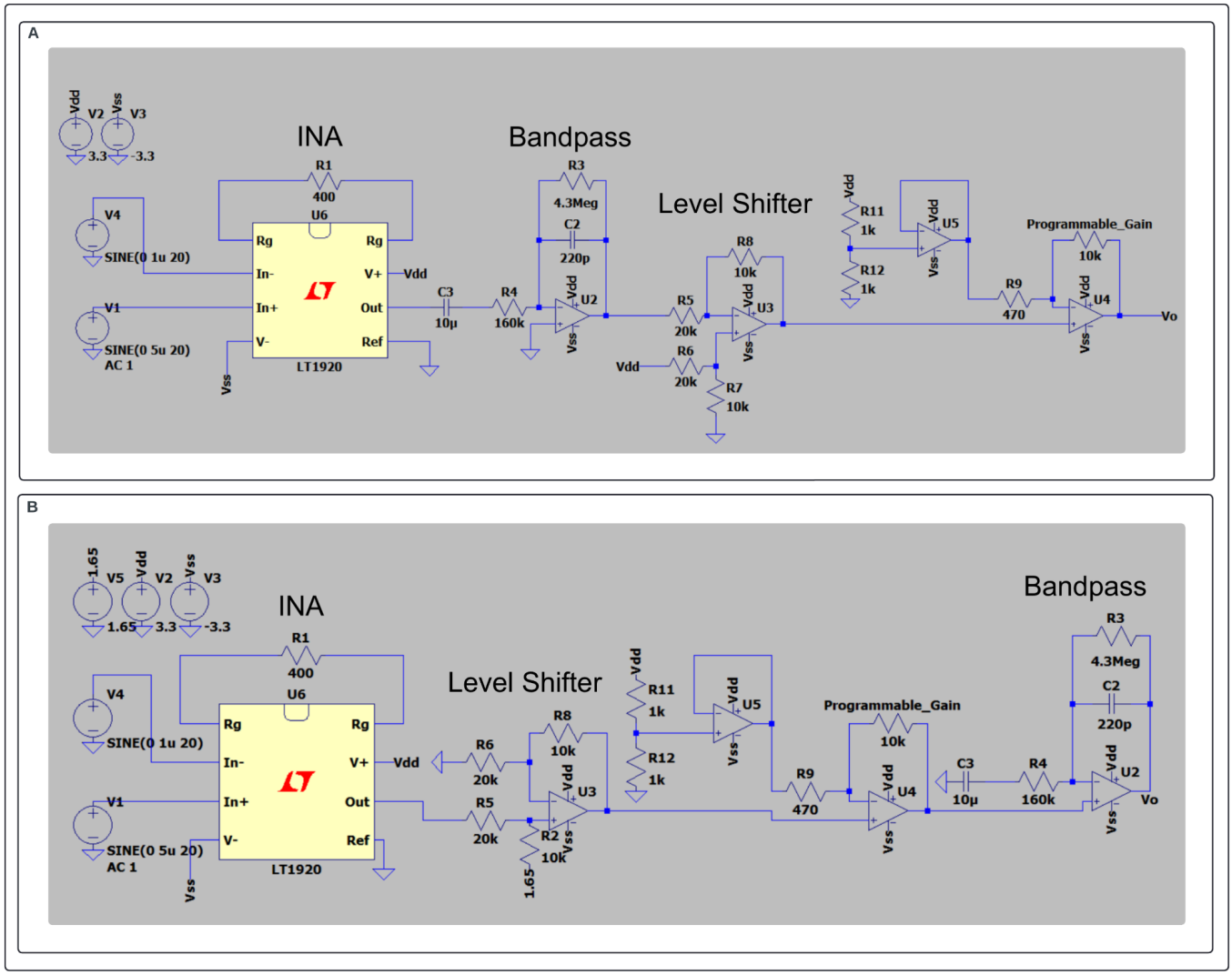


Figure 5: Schematic diagram of the Two Single-channel ADC Configuration. A. Schematic diagram of a single channel of the parallel configuration. **B.** Schematic diagram of a single channel of the series configuration.

Fabrication

Analog Front End

Materials

The heart of the analog front end is the Raspberry Pi RP2040 (Raspberry Pi Foundation, Cambridge, England) in the Raspberry Pi Pico package. It features three on-board ADCs, each samples with 12-bit resolution at 500 ksps, exceeding the 10 ksps minimum requirement (Appendix A). The VBUS pin of the RP2040 is connected directly to the VCC pin of the micro USB, which powers the MCU and the entire analog front end. A microchip TC962EPA (Microchip Technology, Chandler, Arizona) is then used to create VEE. The INA827AIDGKR (Texas Instrument, Dallas, Texas) is used as the instrumentation amplifier since it provides

±40 V input protection, a satisfactory slew rate of 1.5V/μs, and enough -3db Bandwidth of 600 kHz. The multiplexer is the CD74HC4067M96 (Texas Instrument, Dallas, Texas), which allows for the sampling of all signals at a 1kHz rate. The general operational amplifiers consist of TLV9004IDR and TL072CDR (Texas Instrument, Dallas, Texas), which provide four circuits and two circuits, respectively. MCP40D17T-104E/LT digital rheostat (Microchip Technology, Chandler, Arizona) can be programmed to be up to 100kΩ and is coupled with a general operating amplifier to form a variable gain amplifier. Additionally, 100 nF, 10 μF, and 100 μF capacitors are used throughout the PCB as decoupling capacitors. Finally, various resistors, capacitors, and headers complete the circuit.

Methods

The schematics and PCB routing of the two configurations are completed in Altium Designer (Altium, San Diego, California). The final schematic is shown in Figure 6A. Five channels of each configuration are developed, all terminating at a common RP2040 MCU. The first channel of each configuration is tied to a driven right leg circuit for active noise cancellation.

The components of the PCB are then placed and routed. Both sides of the final PCB design are shown in Figure 6B. Signal traces are 0.2 mm wide to minimize crosstalk, and the spacing between traces is as wide as possible. Power traces are 0.5 mm wide to provide low resistance and routed as short as possible. Analog traces are primarily on the front side of the PCB, while digital traces are primarily on the back side of the PCB to minimize digital interference with analog signals. Lastly, the front and back sides are filled with ground (Figures 6C, 6D) with stitching vias distributed in void spaces. A detailed annotated PCB is shown in Figure 7.

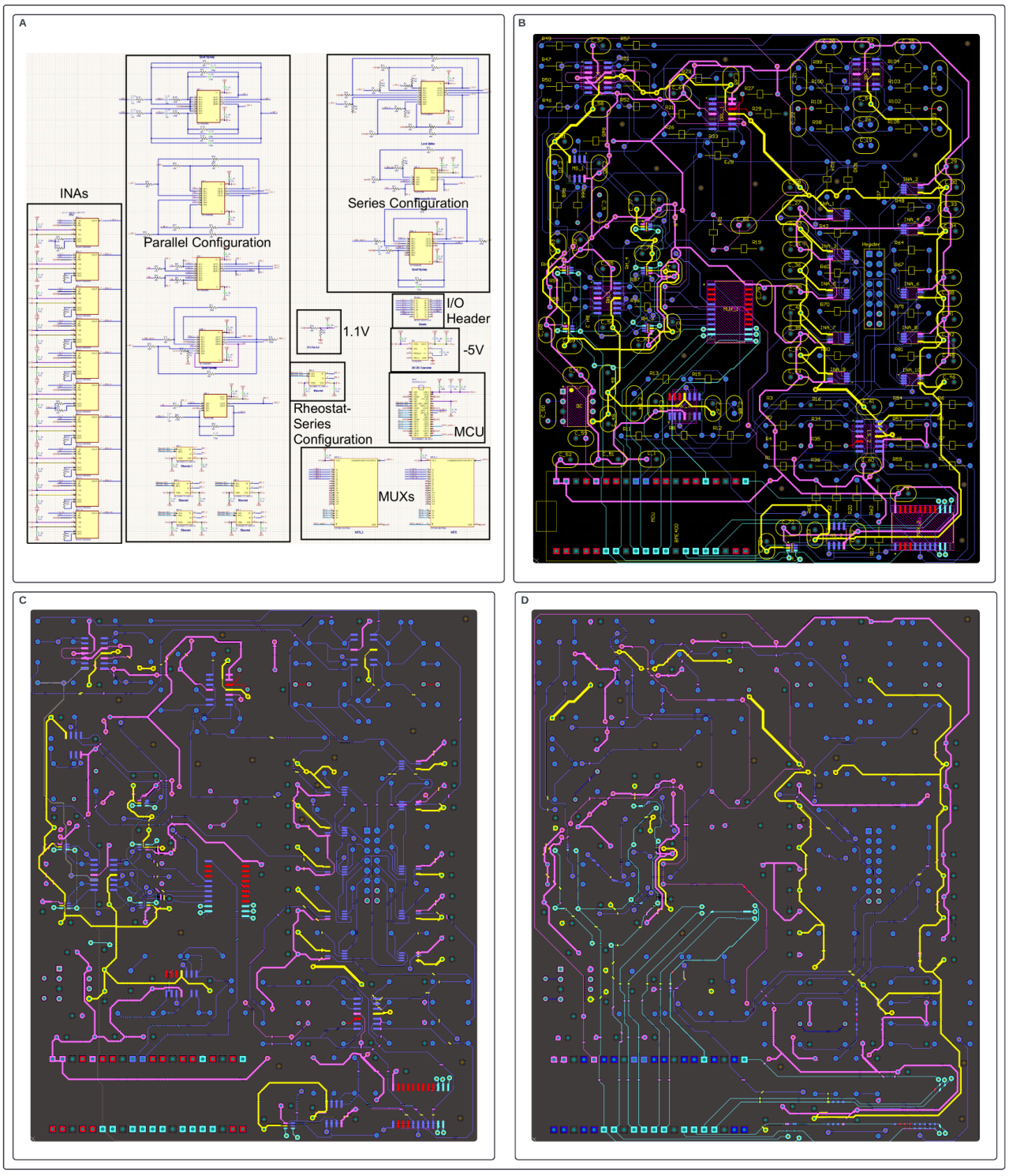


Figure 6: Final Design of the PCB. A. Final schematic diagram of the PCB. **B.** Front side of the PCB without polygon fills. VCC and VEE are colored pink and yellow, respectively. Analog signals are colored purple, and digital signals are colored cyan. **C.** Front side of the PCB with polygon fills and hidden silkscreen. The ground signal is colored grey. **D.** Backside of the PCB with polygon fills and hidden silkscreen.

The PCB is then printed through PCBWay (PCBWay, Shenzhen, China) with parameters specified by Table 3. Lastly, due to timing constraints, two channels of the parallel configuration were populated with components.

Table 3: Manufacturing Parameters of the PCB

Parameter	**Value**
Size (mm)	135.8×114.3
Thickness (mm)	1.6
Minimum Hole Size (mm)	0.3
Material	FR-4 TG 150-160
Layers	2
Via Process	Tenting Vias
Finished Copper (oz)	1
Surface Finish	Hot Air Solder Leveling with Lead
Minimum Track Width (mil)	6
Minimum Track Spacing (mil)	6

Final Prototype

The final PCB prototype is shown in Figure 7. Two channels of the parallel configuration, including the driven right leg circuit, are populated with components.

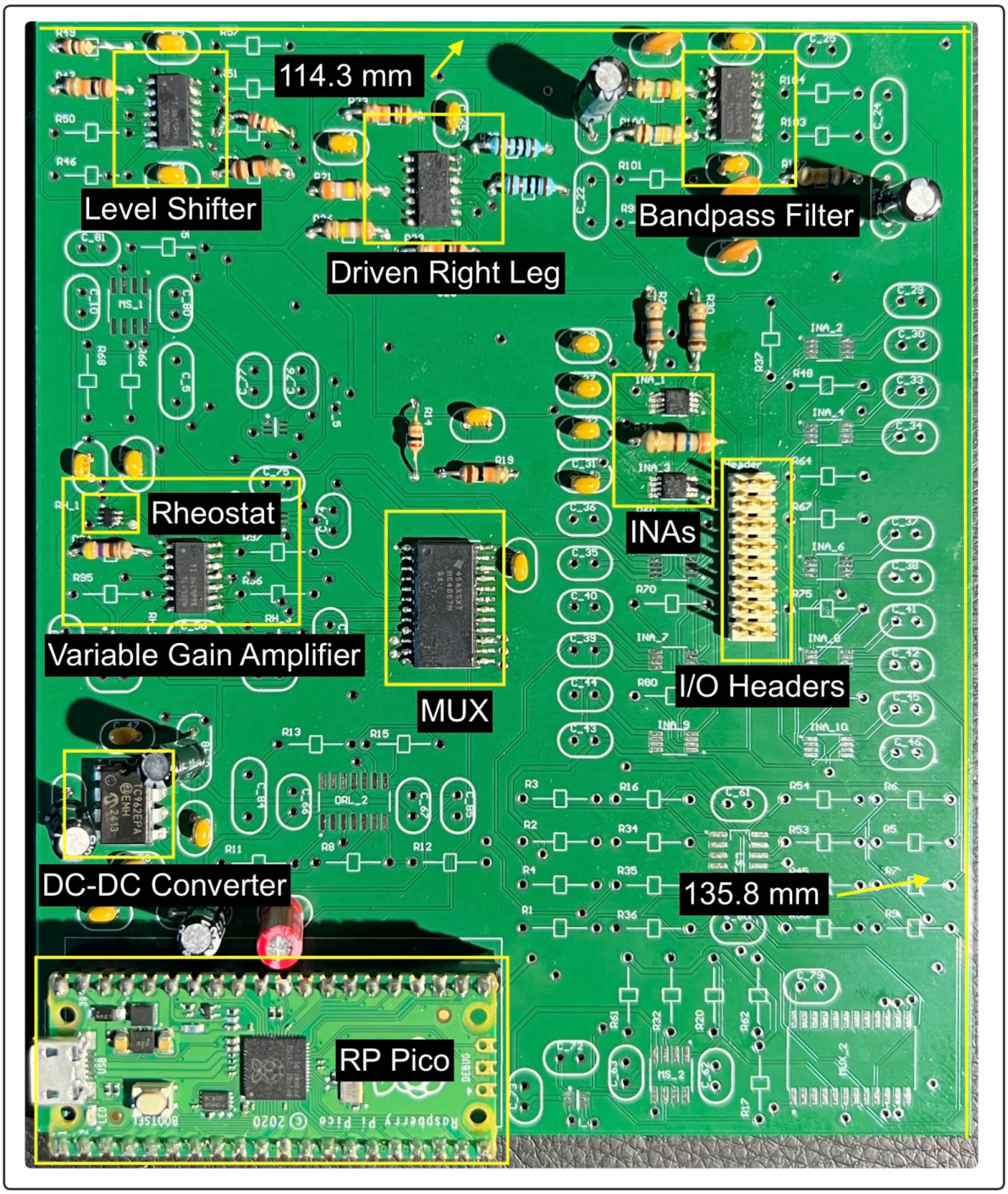


Figure 7: Final Prototype of the Analog Front End

Head cap and Ear Clip

Materials

The head cap is 3D printed with 20 grams of thermoplastic polyurethane (TPU) and 40 grams of support material. The final prototype was printed using Bambu Lab TPU 95A HF with a diameter of 1.75mm +/- 0.003 mm. TPU gives a cost-effective, flexible feeling ideal for putting on and removing the head cap. A flexible material allows stretching and moving of the head cap for slight variations in head size. TPU costs about four cents per gram and is commonly used in 3-D printing, while other flexible, commonly used materials like soft PLA may cost about twelve cents per gram, or flexible uncommon materials like TPS cost around eight cents per gram.

The first design of the ear clip would utilize a torsional spring and 2 grams of polylactic acid (PLA) 3D printed material. The spring utilized was a 45 degree 1.5mm wire diameter spring. The team was able to locate this spring in the biomedical engineering lab free of charge. However, due to fabrication difficulties, the team decided to pivot from this design. The current ear clip design is also 3D printed using approximately 1 gram of polylactic acid (PLA).

Methods

The head cap model is generated using the Neurocaptian plugin for Blender [12]. See Appendix C for detailed instructions. Neurocaptain converted computed tomography (CT) scans to a brain mesh and, eventually, a head cap model. Importantly, a preconfigured version of Blender must be downloaded for Windows 11, and Octave, a scientific and mathematical-focused programming language, must be added to the path. The final prototype was created using the provided “20-24 yr” brain mesh, 4x4 circular holes, and 4.00 thickness.

After this, post-processing in SolidWorks is done to reduce necessary support material. Splitting the model about halfway up the head cap and then creating a spline through the intersected points can create a half-circle edge to later reattach the model after printing. This reduces the necessary support material since the top middle of the head cap does not need to be supported while the bottom outer portion is printed.

The Final prototype was printed using a BambuLab A1 3-D printer using 0.4 mm layer height, 0.62 mm line width, two wall loops, 15% infill density, 500 mm/s travel speed, tree supports at a 30 degree threshold and 360 degree celsius nozzle temperature. This model was sliced in Bambu Studio.

The team originally researched an existing ear clip design that could be purchased and utilized. However, the cheapest EEG ear clip cost approximately 15 dollars. This price would not meet the product design specifications. The preliminary and final prototype were designed using SolidWorks. The preliminary design was created at an angle of 36 degrees to allow for compression of the torsional spring to create tension. The final design utilized the elasticity of the PLA material so when the ear clip is pinched, the clip would return to its original shape and pinch the earlobe. An eight millimeter hole was created on one side of the clip in order to house the electrode.

Final Prototype

The final prototype (Figure 8) of the 3D printed headcap based on the “20-24 yr” brain mesh, fits most heads with a circumference of about 55 cm, is printed from TPU, and accommodates electrodes in the standard

10-20-20 layout with approximately a 7% placement error along the nasion to inion 10% landmarks. The final prototype of the 3D printed ear clip (Figure 9) holds the electrode in place for reference.

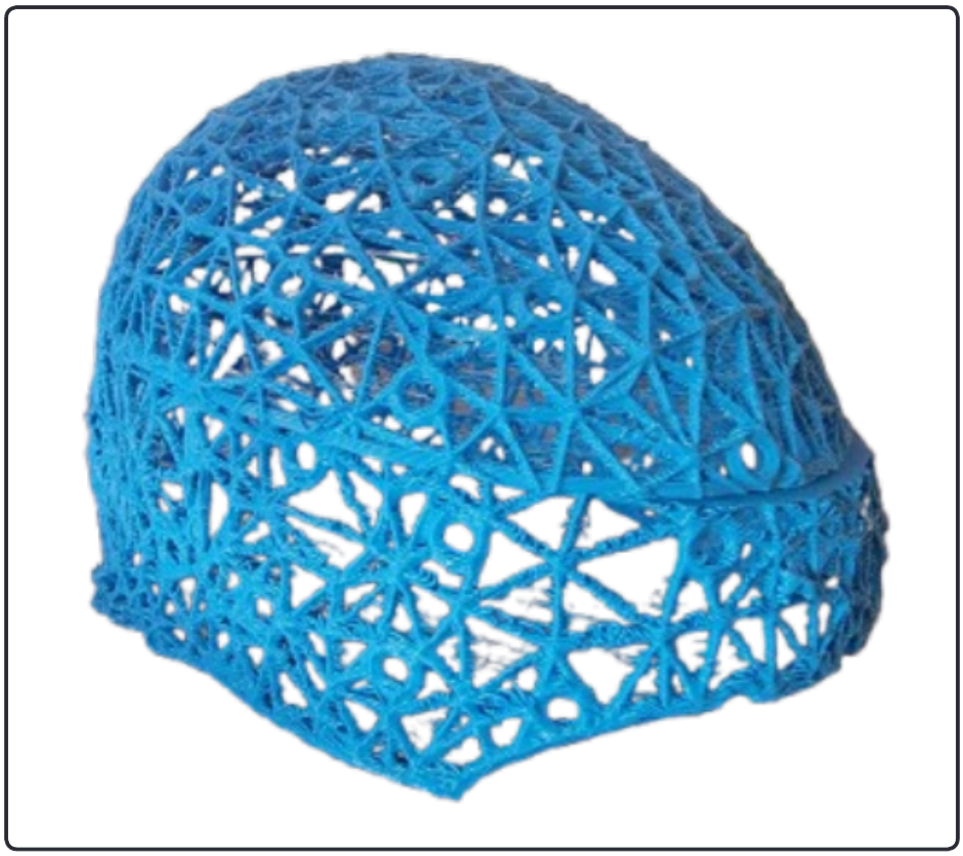


Figure 8: Final Prototype of 3D Printed Headcap

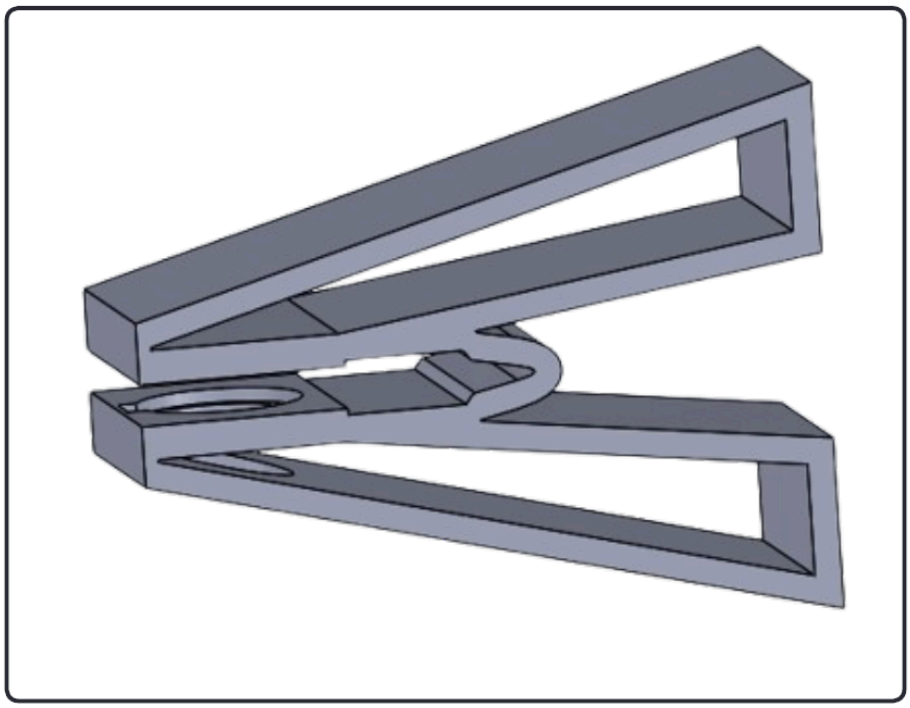


Figure 9: Final Prototype of 3D Printed Ear Clip

Testing and Results

Head cap Testing

To meet the design requirement in the PDS that: (Appendix A) "The system should be accurate and fit users with a maximum horizontal head circumference between 50 to 64 cm" and that the electrode placement fits the standard 10-20-20 layout, the following testing was conducted. A head cap based on a CT scan of a head with 55 cm circumference was created, of the 5 subjects who tried it on, it fit on 2 of them. Showing that there is likely more testing that should be done to see which head sizes will fit inside of this cap, and what sizes would be needed for the highest and lowest parts of the requirement in the PDS. Then, for the 2 heads that the caps fit on, measurements were taken from the nasion to inion to mark the correct position of each 10% landmark, and where the head cap landmark is [13]. From this a percent error was calculated (Appendix D).

$$Absolute\ Percent\ Error\ = \left|\frac{measured\ distance - expected\ distance}{expected\ distance}\right| * 100 \qquad (6)$$

The absolute value of the percent error was used to evaluate the mean and standard deviation of all electrode placements (Equation 6). For the first subject the mean absolute percent error and standard deviation was 5.80% $\pm$ 2.00. While for the second subject mean absolute percent error and standard deviation was 7.29% $\pm$ 13.2. This high standard deviation was likely due to the 10% and 90% landmarks being 41% and 11% off respectively, while all others were between -1.7% and 6.8%. This suggests that readings from the 10% and 90% nasion to inion landmarks may be less accurate for some individuals with this current design and more testing should be done. The head cap did fit for both individuals with head circumferences around 55 cm, but did not for others who were closer to 60cm, suggesting that at least one other larger head cap of this current design will need to be created to meet the needs of the PDS.

Ear Clip Testing

In order for an EEG test to be conducted, the patient must be able to sit comfortably for as long as 20 minutes. The ear clip is one part of the design that could become uncomfortable as it pinches the patient's ear. The team decided to conduct testing to determine how comfortable a patient would be wearing the current ear clip design for the duration of a test. To test this, the team utilized the Borg Discomfort Survey (Appendix E) that measures the perceived rate of exertion and fatigue. The Borg score is rated on a scale of 6 to 20, with 6 corresponding to the slowest perceived exertion and 20 corresponding to maximum exertion. Four patients, 1/ 2 with attached earlobes and 3/4 with detached earlobes, were asked to put on the ear clip and take the survey immediately after application. The participant was then asked to stay seated for ten minutes while keeping their head relatively still for the duration of the test. All four participants brought a computer to complete personal work during the test. After 10 minutes, the participants were asked to take the Borg Discomfort Survey one more time. At the end of this survey, the test was complete and they could remove the clip.

The results from the ear clip testing showed the effectiveness of the design. At the start, all participants rated the ear clip comfort as “Extremely Light” on the discomfort scale or an average of 7.25 (Table 4). At the end of the test, the team did see a 34.5% increase in the mean comfort level of the participants. An increase from 7.25 value to 9.75 was recorded (Figure 10). Throughout the test, some mechanical failures were encountered in the ear clip design itself. The clip started to show signs of permanent deformation. Another observation from the data was that the participants with attached earlobes had an increase in mean discomfort level of 1.5 for the initial and final surveys.

Table 4: Summary of the Discomfort Evaluation of the Ear Clips

Subject #	**Comfort Level After 10 Seconds**	**Comfort Level After 10 Minutes**
1	8	11
2	8	10
3	7	8
4	6	10

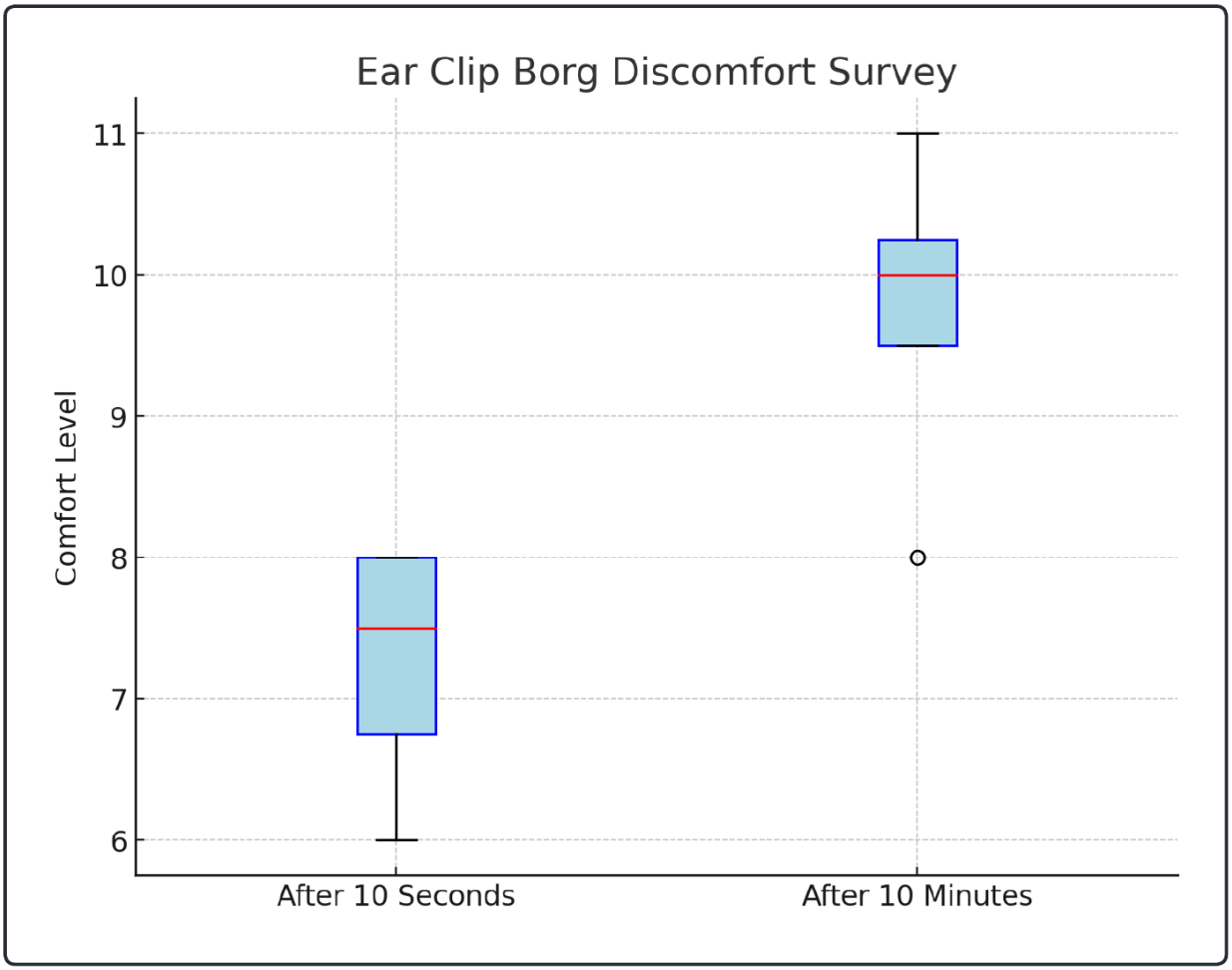


Figure 10: Box Plot Summary of the Borg Discomfort Survey

Simulated Circuit Testing

To begin the testing of the circuit, LTspice® simulations were conducted utilizing both circuits to ensure that the gain and frequency response performed as predicted. The graphs from these simulations are inserted below. Both of these circuits performed as expected, having a gain of 412,500 V/V (Figure 11A), with the ability to increase and decrease due to the variable gain amplifier created by the rheostat. Additionally, the bandpass filter displays a bandpass frequency from .1Hz to 163Hz (Figure 11B), close to the calculated .1Hz to 168 Hz pass frequency calculated using circuit components. To identify the corner frequencies on the bode plot, the frequency values at -3dB from the maximum gain were taken. To calculate these corner frequencies, Equation 1 was used, which is displayed below. Both of these values met the requirements outlined in the PDS, which stated the need for a readable signal and plausible passband. After simulation testing was conducted, as the results were expected, the circuit was approved for fabrication.

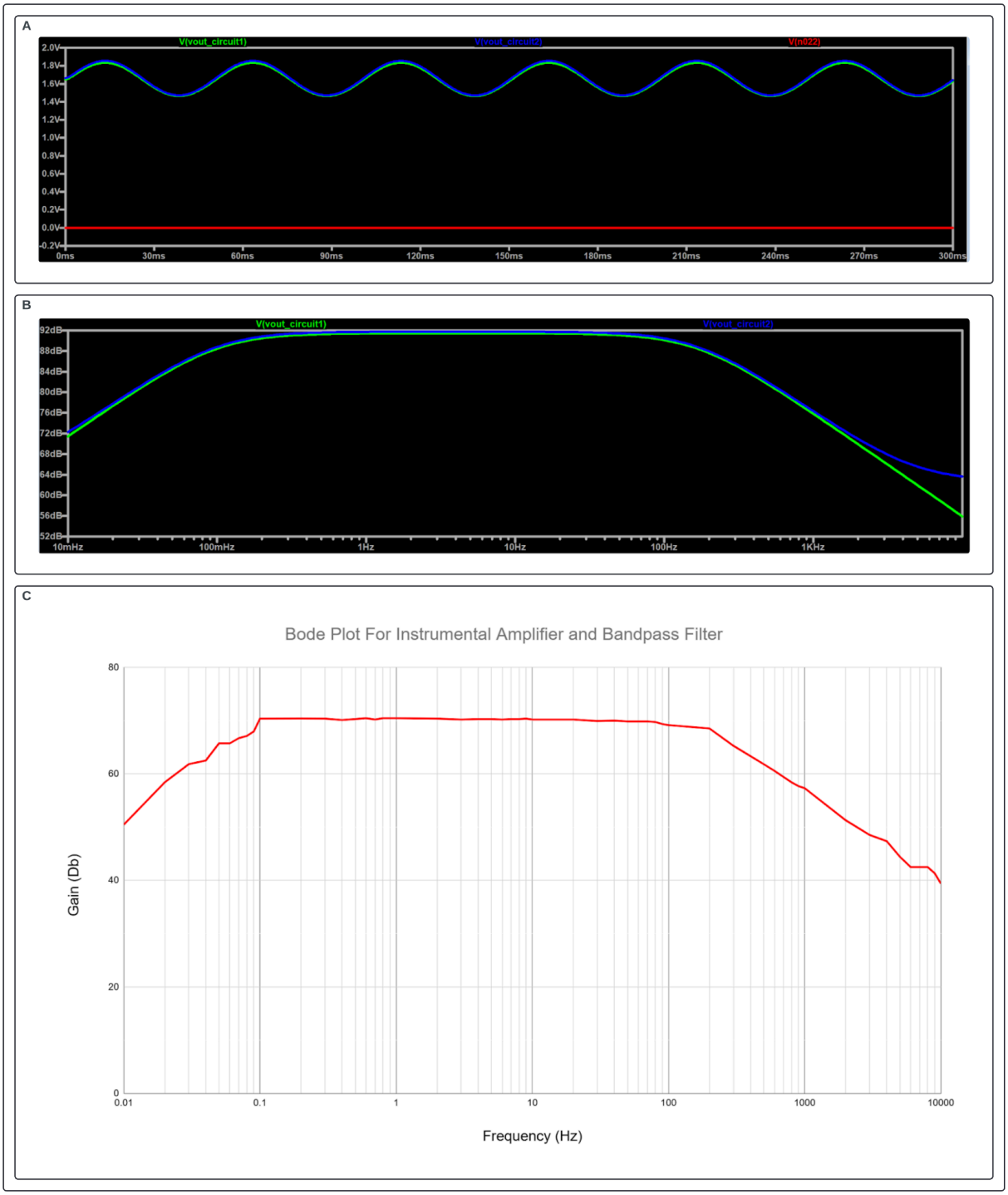


Figure 11: Simulation and Manual Test Results for the Analog Front End. A. Response of both circuits when the input signal is 4 µVolts. Note that circuit one represents the parallel configuration while circuit 2 represents the series configuration. **B.** Bode plot representing the frequency response and gain of both circuits. Note that circuit 1 represents the parallel configuration while circuit 2 represents the series configuration. **C.** Bode plot of the frequency response for the populated third channel within the parallel series configuration. Note that the overall gain occurs at 50.47 dB, which is 333 V/V, and the passband frequency extends from .1Hz to 200 Hz.

Printed Circuit Board Testing

Testing was performed on the circuitry following the assembly. Due to delays in shipping, only two parallel configurations of the circuitry were populated. The first channel of the circuitry was populated. A 20 mV peak-to-peak 100 Hz sinusoidal signal was placed into the header pin of the circuit while the reference electrode was connected to ground. A probe connected to the oscilloscope was set up to allow testing at individual ports.

Then, testing was conducted where each connection was probed individually, starting with the ground and power for the amplifiers. The testing confirmed that the amplifier was grounded, referenced, and powered appropriately; however, an output signal was not being acquired. Upon further investigation, this error was explained by the right leg driven circuit; values within this circuit were not the values expected, creating the potential for error within the circuit. Because of the limited time window, the team conducted testing on the third channel and will debug the first channel in the future.

The third channel, the instrumental amplifier, was populated in the first stage. Testing was then performed to ensure all components were connected correctly, again using the input of a 20 mV peak-to-peak 100 Hz sinusoidal signal. This involved probing each connection, including power and ground at the amplifier, and displaying the output on the oscilloscope. This probing allowed for circuitry functionality after soldering to be verified to allow for resoldering as needed; this also ensured that no components were fried during testing. The gain for the instrumental amplifier was then tested; it was found to have a gain of 33 V/V after repeated testing.

After verifying the instrumental amplifier, the bandpass filter was populated with appropriate components. To allow for suitable gain within this circuit without saturation, the input signal placed into the header was reduced to a 300μV peak-to-peak 100 Hz sinusoidal signal. All of the connections within this amplifier were then confirmed. Following appropriate values, it was decided to procure a frequency response of the amplifier by running a frequency sweeping test to produce a Bode plot. This Bode plot is shown in Figure 10C, with the raw data included in Appendix F.

The maximum gain for the circuit was observed to be 70.47dB or 3333 V/V of gain. This is slightly below the expected value for the first two components, which should have been 3345 V/V. There are a number of factors that can explain the deviation of this value, with the main source being the fact that the input signal was very low. In order to achieve the required input signal for the circuit, the wave generator of the circuit was set to the lowest value, then a voltage divider was created to further reduce the amplitude. This chain of events created some variation, which can appear in the gain. Because of the small input signal, the oscilloscope's measurement might not be reliable, thus the value used for calculation is reliant on calculations from the voltage divider and listed wave generator value. Another reason for the inaccurate gain could have resulted from some variation within the components themselves.

The passband frequency of this amplifier was closer to the expected value, achieving a range of .1Hz-200Hz. This range is acceptable, despite the fact that the 200Hz is on the slightly higher end. This variation could be due to tolerances within the resistors or capacitors themselves. Additionally, there is likely some variation due to the small input signal that is placed into the circuit.

To continue testing, the third channel was populated at the variable gain amplifier. Testing all input and outputs, it was found that the connection to the input was ineffective and not receiving a signal. This is likely due to a manufacturing error, as the signal produced at the output of the bandpass filter was not carried over to the input of the amplifier, despite the pcb trace being the only path for the signal. To solve this problem, a wire

was soldered between the two pins. At this point, testing was terminated, as the pico code was not finished; without appropriate code, the digital rheostat could not function as required.

Future Testing

Due to the timeline of this project, and the extended waiting period for circuit components, testing was not as extensive as planned for the circuitry. Thus, future testing should occur to further confirm various aspects of the circuitry including a Signal-to-Noise Ratio (SNR) and Common Mode Rejection Ratio (CMRR). Testing protocols for both of these can be found in Appendix G and Appendix H.

Signal-to-Noise Ratio (SNR)

The electrodes are first placed on a non-conductive material, e.g., plastic, to collect the baseline noise signal. Then the electrodes are placed on the scalp of a subject according to standard EEG practice and a sample signal is recorded by the microcontroller. The power of the noise and signal are calculated by equation 1:

$$P_{signal} = \frac{1}{N}\sum_{i=1}^{N}\left(V_{signal,i}\right)^2, \tag{6}$$

where Psignal is the power of the signal of interest, N is the number of samples, and V_{signal} is the magnitude of the signal of interest. Then the SNR is given by:

$$SNR(dB) = 10 \times log_{10}\left(\frac{P_{signal}}{P_{noise}}\right). \tag{7}$$

Common Mode Rejection Ratio (CMRR)

The input electrode is connected to a 100 µV peak-to-peak 40 Hz sinusoidal signal, and an additional 60 Hz 10 µV peak-to-peak noise is applied to both the input electrode and the reference. The magnitude of the common mode signal in the output signal is quantified through the Fourier transform. The CMRR is then calculated through equation 3:

$$CMRR(dB) = 20 \times log_{10}\left(\frac{G_{differential}}{G_{common}}\right) \tag{8}$$

where $G_{differential}$ and G_{common} refers to the differential mode gain and the common mode gain, respectively.

Commercial EEG Comparison

It is also important to compare the output of the EEG system to existing commercial solutions to further elucidate its performance characteristics. Through this comparison, we can characterize how our solution performs against the gold standard as a further verification of the system. The detailed protocol is described in Appendix I.

Discussion

From the preliminary data, it is unclear whether the analog front end amplifies the signal accurately enough. This device should be low-cost to allow EEG's to be more widely available. However, this can not come at the expense of inaccurate data. While the acquired signals may not be as clean, they need to be able to

accurately reflect the signals that are occurring within the brain. Initial testing results reveal that signal collection is feasible at low values; adequate gain was also confirmed when the input signal was 300μV. This testing will need to be continued with increasingly lower values to ensure that it holds true as the signal approaches the physiological value of 5-300μV [6]. Additionally, while gain was lower than expected, this value should still be effective in producing a readable result when combined with the gain from the variable amplifier. However, the source of this error needs to be identified before the printing of future circuit boards, to ensure accuracy and reliability of the final board.

As mentioned in the testing section, the circuit's gain was not the expected value. There are several reasons that this could occur. One of these reasons is the input signal; as the oscilloscope is both required to produce and read a small signal value, there is a greater potential for error. The oscilloscope produced the minimum value for the wave generator function, increasing the error probability. Additionally, the signal was run through a voltage divider to further reduce it, creating variability in the results. Due to the large gain experienced, minor collection differences result in a huge difference. For example, inputting a signal of 2mV instead of the 3mV signal that was measured would result in a gain of 500V/V as opposed to 333 V/V. These differences necessitate an accurate signal collection for the value inputted into the circuit; as this cannot be guaranteed with the tools available, a source of error arises.

Another potential source of error arises from the selection of circuitry components. For this project, cost was a major consideration to allow for more accessibility. Thus, to allow for decreased costs, lower-priced components were selected. The trade-off for the price reduction is the tolerance of the components. Due to the decreased price, the chosen components have higher tolerance values. This means resistors and capacitors can have varying values within the circuit, affecting both the gain and corner frequencies. If it is determined through continued testing that the tolerance in these components is causing further issues, higher-priced items can be selected to help eliminate any potential problems. However, a cost-benefit analysis should be employed to ensure that the selection of lower-tolerance components is worth the price increase.

Further issues with this circuit could result from the PCB's manufacturing process. This issue was seen with the trace routing of the output of the bandpass signal to the variable gain amplifier. The inadequate signal had to be corrected with the soldering of an additional wire. As the circuit board is populated, this issue has the potential to continue to occur. Additionally, the cross-talk between signals can pose a difficulty for testing the board. If there is an issue with cross-talk, it will likely occur after populating all channels when there are multiple input signals. The potential for this error will be examined as more channels are populated.

Moving forward, the circuit also needs to incorporate the raspberry pi pico. This will involve writing code that is able to interface with the digital rheostat in order to set the amplifier for the programmable gain. This code will also ensure that the MUX is able to switch signals at appropriate times. Additionally, a printout for the end user must be programmed into this code, including a feature to signal if a possible epileptic episode is erected based on the acquired brainwaves.

Additionally, a design that fits properly on the head is important for the head cap. This test will range from 20-40 minutes, so ensuring that a patient has a properly fitted head cap will allow for improved comfort, a parameter outlined within the PDS specifications in Appendix A. The current head cap design did not fit a number of participants, thus further options need to be pursued. Various sizes of 3-D printed head caps must be printed to allow for suitable technology for all possible participants. These head capes should be tested on various individuals and hair types to ensure that a wide variety of people can use this equipment. If further printing is too expensive, or too many options are needed to fit the variety of individuals, other head cap designs can be reconsidered, such as a design that employs the use of fabric. It is important to note that while specific electrode placement is idealized, current clinical head caps likely result in some variability due to the flexibility

of the material and changing head shape of patients. Because of these variations, small changes in electrodes may be acceptable, however further investigation should be conducted to confirm.

Following extensive testing on the fabricated PCB, another protocol will be created to aid individuals in testing the device independently. This testing can be less intensive, as the device will be known to operate correctly. It will still have to include components to ensure everything is connected correctly. By reducing the total amount of testing that is required, the device will be more accessible to hospitals in need. As many doctors do not have an extensive electrical background, simplifying the testing where possible will open up more opportunities to employ the product and ensure confidence since the doctors can comprehend the test results.

Ethical considerations also need to be taken into consideration when designing this product. This product needs to give consistent, dependable, and reliable results before being used clinically, as it treats patients. This device should also pose no risk to the individuals using it; this includes both the test administrator and the patient themselves. Numerous tests will be conducted to ensure that safety measures are in place for possible events that could happen, including power surges and component failure. The patients must also have informed consent when using this device, which means that a document listing possible outcomes and giving accurate product information must be written up and provided to the patient. All of this will be done prior to connecting anyone to the device.

Conclusions

The team aims to fill the critical need for accessible diagnostic devices for epilepsy by developing a cost-effective EEG system. The team developed a TPU 3D-printed head cap, ear clips to house reference and driven right leg electrodes, and the analog front end on a PCB. The head cap shows a 5.8% to 7.3% mean absolute error in landmark alignment and could not fit on individuals with a head circumference above 60 cm. The ear clips were found to be comfortable among participants, with an initial average Borg score of 7.25 and a 10-minute score of 9.75. However, permanent inelastic deformation was observed during testing. The simulated frequency response of the analog front end (0.1 Hz to 163 Hz) matched its theoretical values and was confirmed by the manual Bode plot. The theoretical gain of the INA (200 V/V) matches the simulation results, but was observed to be only 33 V/V when manually tested.

The head cap shows good land mark alignment for individuals with head size of around 55 cm. However, larger and smaller sizes must be produced to accommodate different head shapes. Although the ear clip was comfortable, its mechanical properties needs to be improved by changing the material or its physical design. Lastly, a sinusoidal signal was able to be amplified by the analog fron end with the correct frequency response; however, the gain of the overall circuits necessitates further investigation. Furthermore, the embedded system must be developed to elucidate the CMRR, PSRR, and SNR of the two circuit configurations to choose the one that is cost-effective and high-fidelity.

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Appendix

Appendix A: Product Design Specifications

Function

Epilepsy is a common chronic neurological disease characterized by abiding recurrent seizures [1]. The most recent WHO report cites 50 million people affected worldwide, whose risk of premature death is up to three times that of the general population [2]. Electroencephalogram (EEG) is the most widely used detection and analysis procedure for epilepsy, which records cortical electrical activity. Identifying EEG patterns and seizure foci is critical for the diagnosis of specific epilepsy syndromes and, consequently, the selection of appropriate therapy [3]. However, 80% of epilepsy patients live in low- and middle-income countries, the majority of which do not have access to EEG systems or treatments [2]. Therefore, affordable EEG systems that can be rapidly and broadly deployed are in critical need.

Client requirements

- A single-channel sampling rate of at least 1 kHz.
- 12- to 16-bit analog-to-digital converter resolution.
- Periodic reading of electrode impedance to detect improper electrode contact.
- Total system cost at or below $100.
- 10-channel analog frontend.
- Driven by wall-plugged power supply.

Design requirements

Physical and Operational Characteristics

Performance requirements

The devices will be used for 20 to 40 minutes per patient per procedure [4]. The frequency of usage is dependent on the medical facility.

Safety

The device must be sanitized between uses, and the skin contact electrodes must be replaced. Since the device involves prolonged skin contact, irritation, discomfort, and allergic reactions are possible. The device consists of active electrical components and wires; thus, it must be carefully handled and not be tampered with while powered on. Furthermore, the device's temperature during operation must not exceed 40 ℃.

Accuracy and Reliability

The system should have a sampling rate of at least 1 kHz per client's requirement. The analog-to-digital converter (ADC) should encode with at least a 12-bit resolution to capture finer details of the EEG waveform. Low impedance, e.g., 5 k**Ω** electrodes, should be used to enhance signal clarity. To improve ease of use, the device should detect improperly connected electrodes. Additionally, signal filtering is required to reduce capacitive coupling effects from power lines and electromyogram interference. Typically, the reliability of a

diagnostic system is measured by its positive predictive value; however, the accuracy of epilepsy classification is critically dependent on monitoring duration and is unrealistic to calculate within the scope of this project [5].

Life in Service

The system must remain operational for 3-4 years with proper daily usage, ensuring durability and consistent performance. It should function effectively within a temperature range of 0-40°C without any drop-off in EEG signal amplitude, as higher temperatures are observed to negatively affect signal quality in existing EEG systems [6]. Additionally, the system must be easy to clean between uses, as it will be exposed to various cleaning products. The head cap should remain functional for 3-4 years with daily cleaning.

Shelf Life

The product should maintain its integrity and functionality in storage for at least ten years at room temperature. It must withstand transportation without any wear or damage and be designed to endure harsh conditions during transit. The product should tolerate storage temperatures ranging from -20°C to 100°C, as it may encounter extreme environments during transportation.

Operating Environment

The EEG cap must ensure consistent and secure contact between the electrodes and the scalp to accurately capture brain signals while maintaining user comfort over extended periods. The materials should be soft, lightweight, and non-invasive, providing a secure yet non-irritating fit. The EEG system should also function reliably in various temperatures typical of indoor and controlled outdoor environments, e.g., 0-40°C. The cap and circuit board should resist sweat, moisture, and mild physical impacts, ensuring long-term durability and accurate signal collection.

Ergonomics

The system should be accurate and fit users with a maximum horizontal head circumference between 50 to 64 cm, similar to other commercially available EEG electrode caps [7, 8]. The system should be effective for users of any hair volume and texture between bald and hair type 1 to 4d [9].

Figure 1. *Examples of hair types*

Size

The entire system should be portable and easy to carry. The cap and electrodes should be able to fit on most children and adults.

Weight

The system should weigh less than 1 lb and cause no neck strain while wearing.

Materials

There are no printed circuit board (PCB) materials restrictions as the device is not intended to operate in extreme environments. Operating temperatures, coefficient of thermal expansion, and electrical characteristics are non-critical factors. Dry electrodes are preferred, typically composed of conductive silicone or gold-plated electrodes, as requested by the client [10]. The head cap should resist cleaning solutions, e.g., ethyl or isopropyl alcohol and chlorine-releasing agents.

Aesthetics, Appearance, and Finish

The cap's design will ensure the patient feels comfortable in the environment. All wires should be as enclosed as the system allows. The circuit board will have a cover to shield the view from the patient. The appearance will be sleek and neutral to avoid any strong aversions. The appearance of the electrodes and the board will be professional in portraying the device's safety.

Production Characteristics

Quantity

One unit is needed for the scope of this project. This unit should be created to be reproducible on a large scale.

Target Product Cost

For one unit, the entire system costs at or below $100.

Miscellaneous

Standards and Specifications

The Code of Federal Regulations Title 21, Volume 8 Chapter 1 Part 882: Neurological Devices provides specific standards concerning electroencephalograms (EEGs) and other commercially distributed neurological devices intended for humans. Sec. 882.1400 states that EEGs are used to measure and record the brain's electrical activity and are classified as a class II medical device [11]. This means they have to follow general regulatory control and special controls, including performance standards, special labeling requirements, and post-market surveillance [12]. They must also go through the 510(k), a premarket submission process that proves the device is similar to one currently operating and showcases that it is safe [13]. To be considered within this classification, the EEG can have recording hardware, monitor, and basic software; however, this does not include electrodes, a complex software analysis system (to either auto-detect or analyze events), or a system with more than 16 electrodes. Additionally, this device is not allowed to be used in sleep studies. EEG

electrode/lead tester is a device used to test the impedance of electrodes. It is classified as a Class I device, along with an EEG signal spectrum analyzer and an EEG test signal generator. Cutaneous electrodes are applied directly to the skin to record or apply electrical stimulation and are classified as a Class II medical device.

In addition to FDA standards, IEEE recommended practice for EEG Neurofeedback Systems details practices that should be abided by [14]. The system must adhere to the IEC 60601-1 Safety and Essential Performance standard to follow safety procedures. The EEG should be sold as a medical device, where the user is trained to operate the equipment properly. System software shall be available to allow all parts of the system to be analyzed as needed. This includes electrodes, which should have an expected lifetime, performance, polarization rate, and long-term stability. Cleaning techniques, application, and impedance checking should accompany these electrodes. Several different specifications should be included for the primary component, as listed in Table 1.

Along with these documents, several ISO and IEC standards are applicable. IEC standard 80601-2-26:2019 details the particular requirements for EEGs' basic safety and performance [15]. ISO standard 22077-5:2021 specifies the format of waveforms created during EEG to support one recording session [16].

***Table 1**: Specifications that must be listed, as stated by IEEE Recommended Practice for EEG [14]*

Amplifier Specifications	**Frequency specifications**	**Analog to Digital Conversion**
Input impedance	Magnitude response	Number of bits, number of channels, and type input/output channel
DC/AC coupling (time constant if ac coupled)	Phase response	Sampling rate
Noise/sensitivity (RMS and/or peak-peak voltage, given bandwidth or application, noise spectrum)	Corner frequency / frequencies	Anti-aliasing filter specification
Signal input range	Decay and rolloff	Resolution, quantization error, and/or least-sig bit size (eg performance over temperature, hysteresis, etc.)
Signal output range	Decibel (dB) attenuation in stopband	ADC technique
Ground type (active/not) or direct reference line noise		Channel-to-channel isolation and digital channel
CMRR		
Gain		
Bandwidth		
Supply voltage/current consumption		
Impedance checking specifications (stimulus, measurement time/duration, absolute accuracy, relative accuracy)		
Amplification		

Customer

The device is tailored for medical clinics in underdeveloped areas; thus, its cost and durability are prioritized. Borth criteria are detailed in this document above. Additionally, the device should be intuitive to use and include detailed instructions in various languages.

Patient-related concerns

Four main patient-related concerns will be addressed:

- **Patient Comfort & Skin Irritation**: Long-term EEG monitoring may cause discomfort or skin irritation, especially due to the electrodes' contact with the scalp. Proper cap design, skin preparation, and using hypoallergenic materials are essential to reduce discomfort and prevent rashes or sores.
- **Movement Restrictions**: Patients must remain relatively still during EEG recording to avoid artifacts from muscle movements. This can be challenging, especially for pediatric or uncooperative patients, leading to inaccurate readings.
- **Infection Risk & Hygiene**: Reusing EEG caps and electrodes poses a risk of infection if they are not properly sanitized between uses. Ensuring strict hygiene protocols and using disposable components when necessary can mitigate this risk.
- **Psychological Stress or Anxiety** Some patients, particularly children or those with certain neurological conditions, may experience anxiety or discomfort during the EEG process due to unfamiliar equipment or the need to remain still for extended periods. Clear communication and a calming environment can help alleviate these concerns.

Competition

Most EEG systems are intended for medical use and are inaccessible to consumers and medical facilities in underdeveloped countries. Although consumer EEG systems with relatively low costs exist, none of the multi-channel systems cost close to the $100 threshold (Table 2). Commercialized products like Neurosky, Muse, and Emotiv often feature non-essential Bluetooth functionalities and auxiliary sensors that contribute to their cost. Their channel count and sampling rate also fall short of the client's requirements. Open EEG's modular EEG system offers the most competitive pricing for its performance. However, its ATmega8 employs a 10-bit ADC with six channels that fail to meet the performance requirements.

***Table 2**: Summary of Existing Consumer EEG Devices*

Product	Channel Count	Sampling Rate (Hz)	Bit Depth	Wireless	Cost (USD)
Neurosky MindWave	1	512	12	Yes	130
Muse2	4	256	12	Yes	300
Emotiv MN8	2	128	14	Yes	400
Emotiv Insight	5	128	16	Yes	500
Emotiv EPOC X	14	256	14-16	Yes	1000
Emotiv Flex Saline	32	256	16	Yes	2000
Open BCI Complete Kit	16	125	24	No	2500

Open EEG	2-6	Up to 15.4k	10	No	200-400

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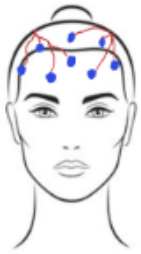
Appendix B: Design Matrix

Table 5: Head Cap Design Matrix

	Store Bought		3D Print		No Head Cap		DIY		
									
	Points out of 5	**Weighted Score**							**Weight**
Cost	0	0	4	80	5	100	4	80	**20**
Safety	5	75	4	60	3	45	3	45	**15**
Accuracy	5	70	4	56	1	14	2	28	**14**
Repeatability	4	56	5	70	1	14	2	28	**14**
Ease of Use	5	65	4	52	2	26	2	26	**13**
Durability	5	60	3	36	4	48	2	24	**12**
Comfort	5	35	4	28	4	28	3	21	**7**
Ease of fabrication	5	25	2	10	5	25	3	15	**5**
Total		**386**		**392**		**300**		**267**	**100**

Cost:

The expected cost to produce one electrode cap. Store Bought is by far the most expensive, with most models being well over $100, No Head Cap requires no additional material so is therefore the cheapest. DIY and 3D Print have the potential to be inexpensive depending on material choice, but do have some cost associated with them.

Safety:

All electrode caps should be safe for use and provide stable electrode connection, while none of these designs provide major risk, Store Bought was most safe since it provides the most protection between the electrodes and head while other designs may be at higher risk for electrodes to come loose.

Accuracy:

The electrode cap design must keep each electrode accurately at the associated biological marker. Store bought was ranked the most accurate since with more material covering the head, strain to cause electrode drift to incorrect locations is minimized by more material. No head cap is the least accurate since it requires the Doctor

to place electrodes manually before each test.
Repeatability:

The design must be able to be constructed and run repeatedly with no dip in performance of the product. The environment, patient, and the person running the test are all factors that could change. Despite these changes, the results should remain consistently accurate. The 3D printed design was ranked the highest because the team would have control over the production of each component unlike the store bought. The no head cap and DIY both ranked lower as these have a much higher chance of human error leading to less accurate results over multiple trials.
Ease of Use:

Ease of use refers to the difficulty for the tester to run the test on the patient. This product needs to be fairly easy to use so that a trained operator can consistently give the test and the patient has no issues during the test. The store bought design ranked highest because the commercial products are tailored to the interest of the consumer, giving it a good chance to be easy to use. The DIY and no head cap ranked lowest as these would require a lot more training on how to create/execute the test.

Durability:

This design must be durable in order to withstand travel, repeated use, and movement as the patient adjusts the product in order to fit the cap to their head. The store bought design was ranked the highest as since these are commercially available, the quality of the product will most likely be higher than our other design ideas. The no head cap scored higher on this metric as there is not much that could be damaged to the product itself. While the DIY and 3D printed designs have a higher chance of human error as well as a design tailored to performance and not durability.

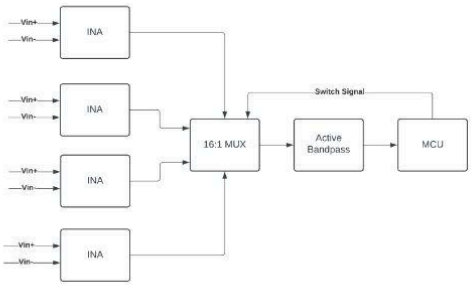
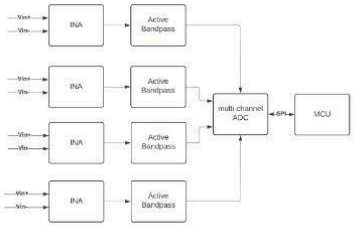
Comfort:

The design must be comfortable enough for the patient to get through the test without any difficulties but the team decided this was not of top priority due to the importance of other factors. The store bought design ranked the highest amongst this metric as since those are typically more expensive the company creating the design has put more effort into the comfort of the product than our other designs. The DIY ranked the lowest as this design would be very simplistic and tailored towards accomplishing the task of running the test accurately without a focus on comfort.

Ease of fabrication:

Ease of fabrication was not weighted as highly as other factors due to most of these products being easy to assemble. The 3D printed design ranks the lowest as this would be the most difficult to fabricate due to the size and structure of the cap itself. The store bought would be easily fabricated as there would be no assembly, the cap would arrive fabricated.

Table 6: Analog Front End Design Matrix

			
	Single-channel ADC + MUX	**Multi-channel ADC**	**Weights**
Cost	26	16	26
Accuracy	16	21	26
Ease of fabrication	20	15	25
Firmware Complexity	5	3	5
Components Availability	14	10	17
Sum	**81**	**65**	100

Cost:

Cost is defined as the listed price of the component on Digikey. The cost for creating the single-channel ADC + MUX costs less to produce, as the multi-channel ADC costs significantly more than the single channel ADC.

Accuracy:

Accuracy is defined as the amount of noise contributed by the individual component. There are less components in the multi-channel ADC, so there is less probability of noise being created. However, neither circuit was given a 5, as the components will generate some amount of noise. This will particularly be true due to the low cost objective; more noise will likely enter the signal acquisition as a result of using cheaper components.

Ease of fabrication:

Ease of fabrication is defined as the amount of time and effort that it takes for the team to fully assemble the system, e.g., soldering, PCB designs. The multi-channel ADC has less individual components, so it will be easier to fabricate.

Firmware Complexity:

Firmware complexity is defined as the associated coding and wiring complexity. The multi-channel ADC received a higher score because of the ease of coding. Creating the code to alternate through each electrode channel is more difficult that reading all of the separate signals at once.

Component Availability:

Components availability is defined as the number of equivalent components available on Digikey. Equivalency refers to the ability of the component being swapped without changes to other components. There are more equivalent swaps for the creation of the single channel circuit, so it was given a higher rating.

Appendix C: Neurocaptain Instructions

1. Download special blender version (see attached zip)
2. Download Octave from here
3. Add octave to system path should look something like this "C:\program files\GNU Octave\Octave-9.2.0\mingw64\bin"
4. Unzip and open blender from step 1
5. Go to edit -> preferences -> from the add in bar, go to the search and search for "Tissue", click the check box, and then search for "NeuroCeption" and click the check box to have both enabled.
6. (Note: this step may not be required in later versions): go to "C:\Users\USERNAME\AppData\Local\Temp" where USERNAME is your username on your PC. create a folder called "iso2mesh-USERNAME" in that folder. Inside the "iso2mesh-USERNAME" folder, create another one called "neurocaptain".
7. Following steps from this video
    1. Drag over bar to show plugin settings
    2. Click neuro Captain bar
    3. Import your file or using one of theirs by clicking Headmesh
    4. select landmarks by clicking tab, and then finding an appropriate point for each landmark by clicking on a point so only that one is orange, then clicking either NZ LPA RPA IZ or CZ, repeat for all landmarks.
    5. Click Create 10-20 Mesh Generation (this step may take some time)
    6. in top right, click the eye on LandmarkMesh so only headmesh is shown
    7. click the headmesh, then click Modify Mesh Density (decide what value to use, about 0.1 looks good)\
    8. Click convert to dual mesh (not working for me right now but will be fixed later)
    9. Choose a cutout shape (circle is likely best for ours)
    10. Click Project 10-20 Landmarks.
    11. Go to the blue tool wrench on the right and click the dropdown and then apply for each item.
    12. Tab and then find a point for the Nz reference, then click Reference Nz
    13. Click cutout Placement
    14. (This is where any adjustments to the model should be made if we want to change anything)
    15. Click Generate Cap

Appendix D Head Cap Testing Data

Table 7: Raw Data from Head Cap Landmark Alignment

Subject 1								Subject 2							
% distance from nasion landmark to inion	Measured Distance (cm)	Expected Distance (cm)	Difference	Percent Error	Mean absolute Percent Error	Median absolute percent error	Standard Deviation	% distance from nasion landmark to inion	Measured Distance (cm)	Expected Distance (cm)	Difference	Percent Error	Mean absolute Percent Error	Median absolute percent error	Standard Deviation
10%	3.5	3.8	-0.3	-7.89	5.80	5.26	2.00	10%	5.5	3.9	1.6	41.03	7.29	1.71	13.2
20%	7	7.6	-0.6	-7.89				20%	8	7.8	0.2	2.56			
30%	11	11.4	-0.4	-3.51				30%	12.5	11.7	0.8	6.84			
40%	14.5	15.2	-0.7	-4.61				40%	15.5	15.6	-0.1	-0.64			
50%	18	19	-1	-5.26				50%	19.5	19.5	0	0.00			
60%	22	22.8	-0.8	-3.51				60%	23	23.4	-0.4	-1.71			
70%	29	26.6	2.4	9.02				70%	27	27.3	-0.3	-1.10			
80%	32	30.4	1.6	5.26				80%	31	31.2	-0.2	-0.64			
90%	36	34.2	1.8	5.26				90%	39	35.1	3.9	11.11			

Appendix E BORG Survey

Table 8: Guide for the Post-Task Borg Survey

Score	Level of exertion
6	None
7	
8	Extremely light (7,5)
9	Very light
10	
11	Light
12	
13	Somewhat hard
14	
15	Hard (heavy)
16	
17	Very hard
18	
19	Extremely hard
20	Maximum exertion

Appendix F: Circuit Testing Data

Table 9: Raw Frequency Response Data from PCB Testing

Frequency (Hz)	Vout	Vin	Gain (INA & BP) V/V	Gain (Db)
0.01	0.1	0.0003	333.3333333	50.45757491
0.02	0.25		833.3333333	58.41637508
0.03	0.37		1233.333333	61.82160939
0.04	0.4		1333.333333	62.49877473
0.05	0.58		1933.333333	65.72613478
0.06	0.58		1933.333333	65.72613478
0.07	0.65		2166.666667	66.71584204
0.08	0.68		2266.666667	67.10775316
0.09	0.75		2500	67.95880017
0.1	0.99		3300	70.3702788
0.2	0.991		3303.333333	70.379048
0.3	0.99		3300	70.3702788
0.4	0.96		3200	70.10299957
0.5	0.98		3266.666667	70.28209642
0.6	1		3333.333333	70.45757491
0.7	0.97		3233.333333	70.19300959
0.8	1		3333.333333	70.45757491
0.9	1		3333.333333	70.45757491
1	1		3333.333333	70.45757491
2	0.99		3300	70.3702788
3	0.97		3233.333333	70.19300959
4	0.98		3266.666667	70.28209642
5	0.98		3266.666667	70.28209642
6	0.97		3233.333333	70.19300959
7	0.98		3266.666667	70.28209642
8	0.98		3266.666667	70.28209642
9	0.99		3300	70.3702788
10	0.97		3233.333333	70.19300959
20	0.97		3233.333333	70.19300959
30	0.94		3133.333333	69.92013198
40	0.95		3166.666667	70.01204701
50	0.93		3100	69.82723388

60	0.93		3100	69.82723388
70	0.93		3100	69.82723388
80	0.92		3066.666667	69.73333145
90	0.88		2933.333333	69.34722835
100	0.86		2866.666667	69.14754393
200	0.8		2666.666667	68.51937465
300	0.55		1833.333333	65.2648287
400	0.44		1466.666667	63.32662844
500	0.37		1233.333333	61.82160939
600	0.32		1066.666667	60.56057447
700	0.28		933.3333333	59.40073553
800	0.25		833.3333333	58.41637508
900	0.23		766.6666667	57.69213163
1000	0.22		733.3333333	57.30602852
2000	0.11		366.6666667	51.28542861
3000	0.08		266.6666667	48.51937465
4000	0.07		233.3333333	47.35953571
5000	0.05		166.6666667	44.43697499
6000	0.04		133.3333333	42.49877473
7000	0.04		133.3333333	42.49877473
8000	0.04		133.3333333	42.49877473
9000	0.035		116.6666667	41.33893579
10000	0.028		93.33333333	39.40073553

Appendix G: PSRR Testing Protocol

PSRR = 20 log (Δvin/Δvout)

Materials

1. AC+DC network summing device
2. Oscilloscope (ideally one that can automate frequency sweep)

Protocol

1. Connect 5V DC to the summing device and an AC 60 Hz source with 100mV PtP
2. Connect the recording electrode and reference to 1V DC
3. Observe the PtP ripple amplitude at Vout
4. calculate PSRR

Appendix H: CMRR Testing Protocol

Stage 1 - Testing without Mux

1. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.
2. Hook up the input of the first instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes of the first instrumental amplifier.
3. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.
4. Apply a 20Hz 100 µV sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 µV sine wave to the wave generator that is attached to both the input and reference input.
5. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.
6. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.
7. Perform calculations using the equation $CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}})$, where the $G_{differential}$ is the value of the output at 20Hz, and G_{common} is the value of the output at 60Hz. Both the $G_{differential}$ and G_{common} should be expressed in voltage.
8. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.
9. Repeat this protocol with 5Hz, 10Hz, 15Hz, 25Hz, and 30Hz all replacing the 20 Hz signal, keeping the signal amplitude at 100 µV.

Stage 2 - Testing with Mux

10. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.
11. Hook up the input of the instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes. All of the inputs for the instrumental amplifier should receive the same signal, as should all of the reference nodes.
12. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.
13. Apply a 20Hz 100 µV sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 µV sine wave to the wave generator that is attached to both the input and reference input.

14. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.
15. Inspect the data and note anything of significance that could account from the addition of the mux. This can include spikes or lapses in data.
16. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.
17. Perform calculations using the equation $CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}})$, where the $G_{differential}$ is the value of the output at 20Hz, and G_{common} is the value of the output at 60Hz. Both the $G_{differential}$ and G_{common} should be expressed in voltage.
18. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.
19. Repeat this protocol with 5Hz and then 30Hz replacing the 20 Hz signal, keeping the signal amplitude at 100 μV.

Appendix I: Commercial EEG Comparison

Material

- Tucker-Davies Technology recording cart
- EEG testing board
- 5-6 gold cup electrodes
- electrode gel/cream
- abrasive gel/paper towel
- tape measure
- marker
- gauze

TDT setup

- The recording and reference electrodes are attached to the TDT amplifier
- recording software is opened and ready to record

PCB setup

- The EEG PCB board should be connected to a computer via a micro USB cable.
- The recording, reference, and DRL electrodes are attached to the board.
- Appropriate recording software/terminal is opened and ready to record

Procedure

1. Identify attachment location according to the 10/20 standard.
    1. Use a tape measure to drape across the head to coincide with the sagittal plane.
    2. Make sure the tape measure begins at the nasion and ends at the inion.
    3. Mark the skin at 10% of the length from the nasion (Fp1).
2. Clean the skin at the location and use abrasive gel or paper towel to reduce impedance.
3. Apply electrode gel to the gauze.
4. Apply adequate electrode gel to the cup electrode and place the stem of the electrode on the gelled gauze
5. Press gently on the skin
    1. repeat for the two recording electrodes and others
6. begin recording

7. end recording after 5 mins
8. align recordings
9. adjust for sampling frequency if there is any difference
10. calculate dB error
    1. 20log(ground truth/PCB)
11. calculate variance and mean