Affordable Diagnostic EEG System for Viral-induced Epilepsy

Richard Yang[1,2], Ellie Dingel[1], Mark Rice[1], Elliott Harris[1], Amit Nimunkar[1], and Brandon Coventry[3,4]

[1]Department of Biomedical Engineering, University of Wisconsin-Madison, Madison WI 53701 USA

[2]Department of Computer Sciences, University of Wisconsin-Madison, Madison WI 53701 USA

[3]Department of Surgery, University of Wisconsin-Madison, Madison WI 53701 USA

[4]Department of Neurological Surgery, University of Wisconsin-Madison, Madison WI 53701 USA

* Corresponding author: Brandon Coventry, coventry@wisc.edu

Abstract*–Epilepsy is a prevalent neurological disorder affecting approximately 50 million people worldwide, with 80% of cases occurring in low- and middle-income countries where access to diagnostic tools like electroencephalograms (EEGs) is limited. Conventional EEG devices are prohibitively expensive, restricting early diagnosis and treatment planning. This study presents the development of an affordable, portable, and reliable 10-channel EEG system for diagnosing viral-induced epilepsy, with a targeted production cost of under $100. The system comprises a custom-designed printed circuit board (PCB) for signal acquisition and amplification, a 3D-printed head cap for electrode placement, and an embedded system for real-time signal processing and data transmission. The analog front-end utilizes a Raspberry Pi RP2040 microcontroller, an instrumentation amplifier, and a multiplexer-based architecture to enhance signal fidelity while minimizing switching artifacts. The system achieves an average common mode rejection ratio of 65.1 dB and signal-to-noise ratio of 24.5 dB and captures evoked biopential from blinking. A GUI can display all ten channel in realtime with configurable parameters. The embedded system timing achieves a standard deviation of 0.24 µs in sampling period. The electronics component (not including the PCB) cost $42. Future work will focus on refining the head cap design for broader fitment, improving ear clip durability, and optimizing the analog circuitry for enhanced signal quality. This EEG system costs less than $100 and has the potential to significantly improve epilepsy diagnostics in resource-limited settings, enabling earlier intervention and better patient outcomes.

***Keywords*–Epilepsy, low-cost instrumentation, embedded system**

I. INTRODUCTION

It is estimated that 1 in 26 Americans develops Epilepsy at some point in their lifetime. Epilepsy is a neurological disorder that causes sporadic seizures affecting 50 million people worldwide [1]. Various treatments exist for Epilepsy, such as anti-seizure medications (AEDs), ketogenic diets, seizure-preventing devices, and surgery [2], [3]. However, diagnosis of the sub-type of Epilepsy is required before a treatment plan can be devised. The primary way to detect Epilepsy without observing recurring seizures is through an electroencephalogram (EEG) [4]. The EEG system is placed on the patient's scalp and is used to detect the electrical impulses in the human brain. Currently, EEG devices are expensive and difficult to obtain. Medical-grade EEG systems cost tens of thousands of dollars, and open-source projects are still prohibitively expensive. OpenBCI, a partially open-source project known for its brain-computer interface devices, offers an eight-channel biosensing board, EEG cap, and electrodes for $2,578[5]. Although this device may be effective, areas without the necessary resources could not afford a stock of these devices to detect and diagnose epilepsy. 80% of epilepsy patients live in low- and middle-income countries, the majority of whom have access to treatment but not diagnostic equipment [6]. Other innovations, such as the Bionode - a wireless, implantable device used for neuromodulation stimulation developed at Purdue - demonstrate the ability to fabricate more affordable devices by using off-the-shelf components [7]]. Similarly, this project aims to create a reliable, accurate, and inexpensive EEG device. The product must receive, process, and display signals from ten channels in a format that a medical professional can easily interpret.

EEG signals originate from the synchronized electrical activity of pyramidal neurons in the cerebral cortex [8]. When neurons communicate, they generate postsynaptic potentials—small voltage changes that occur when neurotransmitters bind to receptors on the neuronal membrane. These potentials propagate through neural tissue via volume conduction and combine to form electrical fields that can be measured at the scalp. Individual action potentials are too brief (1-2 ms) to be detected by scalp electrodes; instead, EEG primarily captures the summation of slower postsynaptic potentials (10-250 ms) from thousands to millions of neurons firing in synchrony [9]. The amplitude of these signals is quite small, typically ranging from 5 to 300 microvolts when measured at the scalp, necessitating significant amplification for clinical interpretation. Different frequency patterns in these signals correspond to various brain states and neurological conditions, making EEG valuable for diagnosing disorders like epilepsy [9].

Epilepsy is a brain disorder characterized by abnormal neuron activity, leading to misfires in the brain and resulting in seizures. Two or more seizures with an unknown cause is classified as Epilepsy [10]. Various conditions and circumstances can trigger epilepsy to develop, one of which is viral encephalitis. This condition, characterized by acute inflammation in the brain, increases the risk of developing epilepsy [11]. Viral encephalitis is more prevalent in low and middle income countries, as diagnostic equipment and testing is limited [12].

Conventionally, EEG uses scalp electrodes that record a variety of active neuronal potential fluctuations. The potentials are aggregations of neuronal action potentials [9]. These recordings usually range from 0.5 to 100 Hz and their amplitudes range from 5 μV to 300 μV [9]. EEG can detect miscommunications between neurons. These channels that detect those miscommunications will tell the physician that the patient may have epilepsy. Using more channels across different brain regions can give a higher chance of detecting these disruptions in brain activity. One study found that Epilepsy affects the hippocampus, amygdala, frontal cortex, temporal cortex, and olfactory cortex most often. However, disruptive activity can be detected across many brain regions [13]. This justifies the constraint of 10 channels rather than eight or fewer channels, giving a higher chance of detection.

Neurodiagnostic tests like EEG are challenging to perform in less fortunate areas. A study completed by the American Academy of Neurology says that in most low-income countries surveyed during the study, only the top 10% or 20% of the population could afford tests below catastrophic levels. In surveyed lower-middle-income countries, >40% of the population, on average, could not afford neurodiagnostic tests [4]. This is in stark contrast to high-income countries like the United States, and Western Pacific World Health Organization regions, where more than 70% of the total population can afford EEG tests [4]. The Diagnostic EEG device intends to make testing more accessible for low- and middle-income countries and production cost should remain under 100 dollars. This device must also be compatible with various head shapes and sizes. The team found that the 50-64 cm circumference range would capture all regular occurring head sizes [14]. The device must remain in operation for 3-4 years without a dip in performance. The device must be able to be transported, stored, and implemented in a variety of temperatures depending on the environment.

This project also includes the processing of low-amplitude signals from the brain. This consists of filtering and amplifying the signal. The design must be cost-effective and easy to fabricate. Filtering 60 Hz power line noise is vital in any environment where capacitive coupling from the powerline and other electrical interferences exist. One commonly used filtering technique is a bandpass filter, which uses a circuit of varying electrical components to achieve a calculated sampling frequency. Instrumentation amplifiers are critical elements extensively used for input buffering and high voltage gain [15].

II. SYSTEM DESIGN

The system consists of four components, the electrical circuit, the embedded system, the EEG headcap, and a protective case.

A. Electrical Circuit

The electrical circuit acquires, amplifies, and processes ten EEG channels. The frequency ranges of interests are delta (0.5 to 4 Hz), theta (4 to 7 Hz), alpha (8 to 12 Hz), beta (16 to 31 Hz), and gamma (36 to 90 Hz) [16]. All of these frequencies are captured and amplified by the circuit. The sampling frequency is 1 kHz per channel.

The PCB is developed in Altium Designer (Altium, San Diego) to satisfy the above requirements while minimizing switching artifacts. Each channel has a dedicated instrumentation amplifier (Figure 1A), bandpass filter (Figure 1B), level shifter (Figure 1C), and variable gain amplifier (Figure 1D). The variable gain amplifier is composed of a potentiometer with a variable resistance. All the channels then terminate at the multiplexer (MUX) and are read directly by the ADC. Since each channel is independent from one another, they are ready to be sampled at any given time, and the only switching artifact produced is from the MUX itself. Ten channels of this design are printed on a PCB (PCBWay, Shenzhen, China) for testing.

A block diagram of the circuit is shown in Figures 2. The bandpass filter is tuned to corner frequencies 0.1 Hz and 168 Hz with Equation 1.

$$f_c = \frac{1}{2\pi RC} \tag{1}$$

The gain of the INA is given by Equation 2 and has a value of 227V/V/. The bandpass filter has a gain of 26.9V/V and the level shifters' gain is 0.5 V/V. The variable gain amplifier has a minimum gain of 1 and a maximum gain of 31.3V/V. Thus, the total gain of the amplifier ranges from 3,053 V/V to 95,563 V/V.

$$5 + \frac{80k\Omega}{R_G} \tag{2}$$

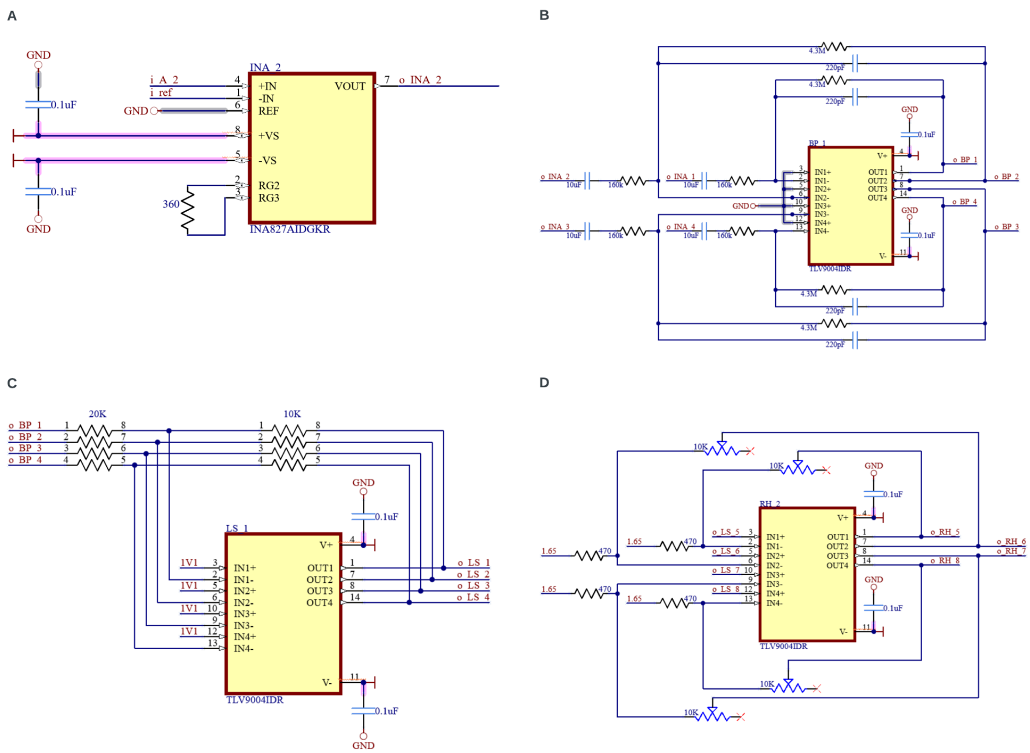

Figure 1: Schematics of selective circuit elements. A. Schematic of the Instrumentation amplifier circuit for the second channel. i_A_2 is the input signal for the second channel, i_ref is the common reference signal, and o_INA_2 is the output signal. B. Schematic of the first Bandpass cluster. Four bandpass channels are located on this operational amplifier. o_BP_n is the bandpass output for the nth channel. C. Schematic of the first level shifter cluster. Four level shifter channels are located on this operational amplifier. o_LS_n is the output for the nth level shifter channel. “1V1” is a buffered 1.1 V DC signal generated onboard. D. Schematic of the first variable-gain amplifier cluster. Four channels are located on this operational amplifier. o_RH_n is the nth output of the variable-gain amplifier channel. “1.65” is a buffered 1.65 V DC signal generated onboard.

A driven right leg (DRL) circuit is implemented within channel one of the analog front end. This design feature aims to reduce the common-mode interference that will be experienced. The common mode signal is acquired through an averaging resistor network at the input to channel one, which is then buffered, inverted, and amplified. A 20 kOhm resistor is placed at the output of the DRL output to limit current.

The heart of the analog front end is the Raspberry Pi RP2040 (Raspberry Pi Foundation, Cambridge, England) in the Raspberry Pi Pico package. It features three on-board ADCs, each samples with 12-bit resolution at 500 ksps, exceeding the 10 ksps minimum requirement (Appendix A). The VBUS pin of the RP2040 is connected directly to the VCC pin of the micro USB, which powers the MCU and the entire analog front end. A microchip TC962EPA (Microchip Technology, Chandler, Arizona) is then used to generate -3.3V. The INA827AIDGKR (Texas Instrument, Dallas, Texas) is used as the instrumentation amplifier since it provides ±40 V input protection, a satisfactory slew rate of 1.5V/µs, and enough -3db Bandwidth of 600 kHz. The multiplexer is the CD74HC4067M96 (Texas Instrument, Dallas, Texas), which allows for the sampling of all signals at a 1kHz rate. The general operational amplifiers consist of TLV9004IDR and TL072CDR (Texas Instrument, Dallas, Texas), which provide four circuits and two circuits, respectively. The PT01-B120D-B103 (Same Sky, Portland, Oregon) is a potentiometer with a variable resistance ranging between 1 and 1,000kΩ. This potentiometer is coupled with a general operating amplifier to form a variable gain amplifier. Additionally, 100 nF, 10 µF, and 100 µF capacitors are used throughout the PCB as decoupling capacitors. Resistors and capacitors are used to achieve the passband and gain specified above. Two rows of headers are added for the 10 input signals and act as breakout-pins for ground and reference.

The components of the PCB are then placed and routed. Signal traces are 0.2 mm wide to minimize crosstalk, and the spacing between traces is as wide as possible. Power traces are 0.5 mm wide to provide low resistance and routed as short as possible. Analog traces are primarily on the front side of the PCB, while digital traces are primarily on the back side of the PCB to minimize digital interference with analog signals. Lastly, the front and back sides are filled with ground with stitching vias distributed in void spaces. The PCB is then printed through PCBWay (PCBWay, Shenzhen, China) with parameters specified by Appendix H.

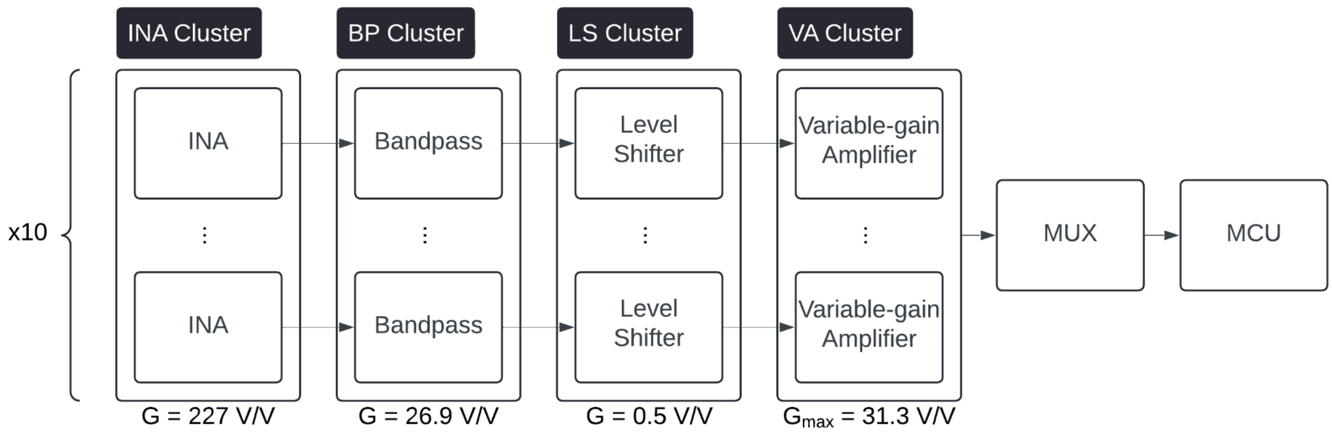

Figure 2: Block diagram of the analog front end. 10 replicas of the instrumentation amplifier (INA), bandpass (BP), level-shifter (LS), and variable-gain amplifier (VA) chain are present in the design. Each chain is dedicated to a single channel. This cluster of chains terminates at the multiplexer (MUX) which is connected to the microcontroller (MCU).

The Embedded system controls on board electronics, reads analog signals and digitally sends those signals over USB. It accommodates up to 10 channels, samples each channel at 1 kHz and runs on the RP2040. The RP2040 connects with and controls the CD74HC4067M96, and reads the output from that. It was designed using the C programming language, programmed within Visual Studio Code using the Raspberry Pi Pico pluggin. The embedded system first, initializes GPIO pins, and sets an interrupt function at the number of channels multiplied by 1 kHz sample rate. After this, inside the interrupt function, the embedded system reads the analog signal from the output of the CD74HC4067M96, assigns it to its appropriate channel and then cycles through to switch the CD74HC4067M96 to the next channel. This operation order maximizes the time between switching channels and sampling that channel and ensures that the CD74HC4067M96 has sufficient time to stabilize (Figure 3). Once all 10 channels have been read it begins to fill a buffer array, once full it sends this data over USB and switches to filling another buffer array (Figure 3).

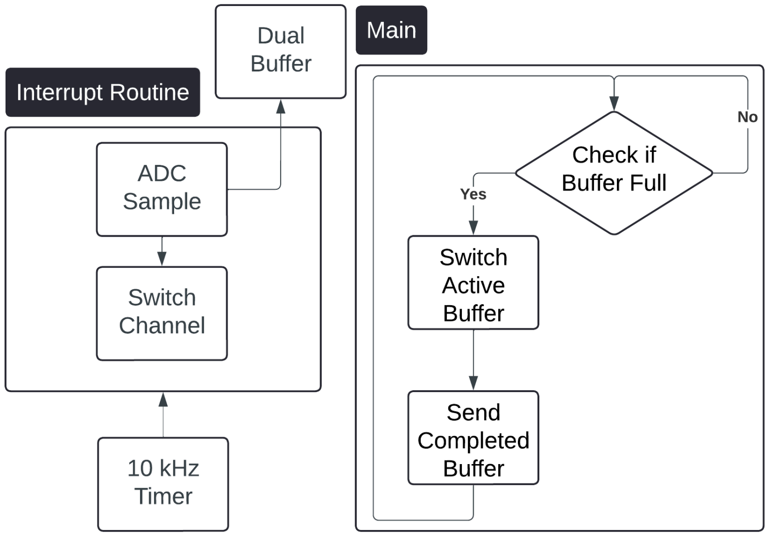

Figure 3: Block diagram of the embedded system.

B. Head Cap and Ear Clip

The design of the ear clip utilizes the mechanical properties of PLA as a spring. This allows the design to adjust to a variety of earlobe thicknesses and can be easily changed for different electrodes. This design allows a print in place ear clip to be easily made from about 12 grams of PLA, costing about $1.44. Once the ear clip was 3D printed, the electrode had to be attached to create a stable connection and ground the system. The adhesive, ethyl 2-cyanoacrylate, was utilized to attach a single electrode to the base of the ear clip shown in Figure 4B.The final head cap prototype (Figure 4A) was developed using a third-party skull cap [9]. After discussions with TECH collaborators, it was concluded that the exact positioning of electrodes was less critical than maximizing the surface area they cover. Since seizures can originate from various regions of the brain, the team opted for a non-specific layout of 10 electrodes strategically distributed to cover a broad area of the scalp. To attach the electrodes, small incisions were made in the skull cap, allowing the electrodes to slide into the fabric. Each electrode then snaps into a crease that helps hold it securely against the head.

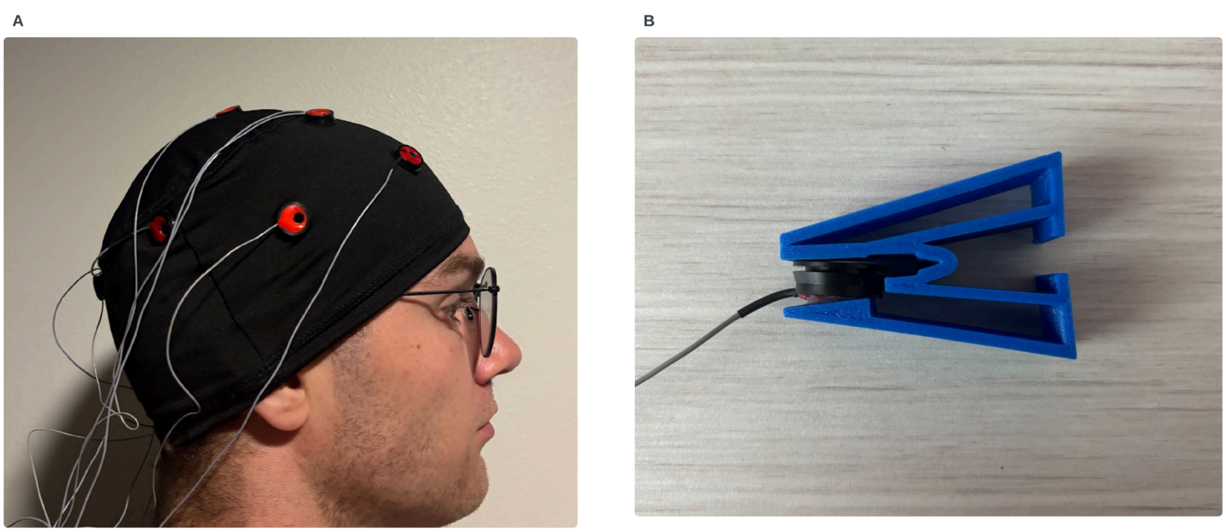

Figure 4: Headcap prototypes. A. Final Prototype of 3D Printed Headcap. B. Final Prototype of 3D Printed Ear Clip

C. Graphic User Interface

The graphic user interface (GUI) is programed in Python 3.13 with PyQtGraph. It displays all 10 channels in realtime with the possible command line configurations listed in Table 1.

Serial communication is handled by the pyserial package. On startup, the application attempts to open the specified serial port at the user-defined baud rate. The serial input must be ASCII lines containing 10 comma-separated floating-point values. Inputs not conforming to this format are discarded. Incoming samples are appended to per-channel ring buffers, each fixed to the user-specified history length. Simultaneously, raw values are written to a CSV file. To minimize I/O overhead, the writer flushes buffers only every 100 samples. On startup, if a CSV file with the default path already exists, the user is prompted to erase or preserve the file.

The GUI window arranges ten individual plots in a grid (default five rows by two columns). Each subplot is labeled with its channel index, y-axis (voltage), and an x-axis label indicating sample history. To maintain high frame rates, the peak-preserving downsampling method is applied when updating plot lines. Per-channel statistics (min, max, average) and global statistics (total samples, elapsed time, sample rates) are updated upon every ten plot updates. An example of this interface is shown in Figure 5.

Table 1: command line argument for the Python GUI

Command line argument	Description
‘--port’	Name of the serial port to read from
‘--baud’	baud rate
‘--history’	Number of samples to be displayed on any given frame
‘--csv’	CSV file output path
‘--min’	Y-axis minimum in volts
‘--max’	Y-axis maximum in volts
‘--layout’	Plot layout in strings, for example ‘5x2’
‘--update-rate’	Graph update rate in Hz

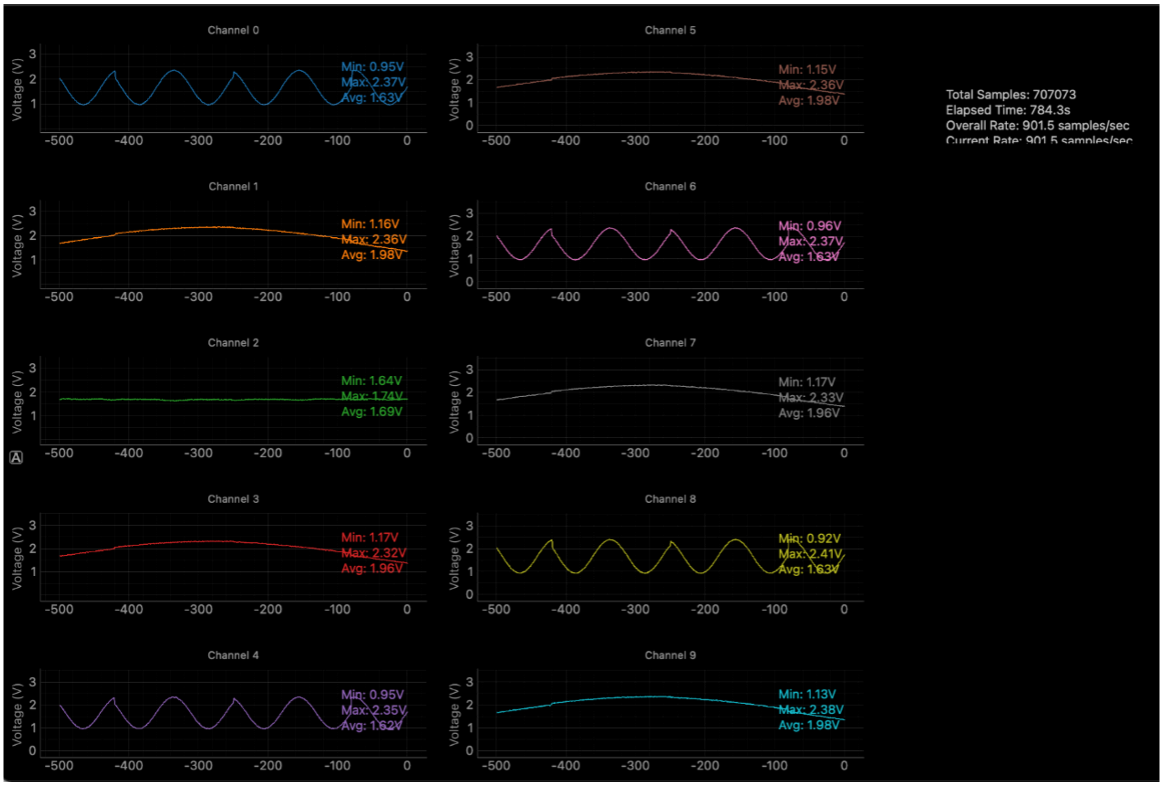

Figure 5: example of the GUI displaying 10 channels in realtime

D. Circuit Board Case

The 3D printable case is made to protect electronics during use, allow a microUSB cable to plug into the RP2040 for power and data, and provide an open area to access electrode headers and gain potentiometers. It can be printed from about 100g of PLA costing about $12.00, although other materials can be used. It is printed in 2 parts. First, a case that uses 4 6mm nylon M3 male screws costing about $0.13, any material M3 screws should work. And a cap that has press fit clips on 3 sides to hold on during use. The complete CAD design is shown below in Figure 6 including the gain potentiometers.

Figure 6: CAD design of Circuit Board Case

III. System Verification

A. Circuit Verification

Circuit verification is divided into four sections: basic verification, electrical characterization, evoked biopotential recording, and DRL verification (also known as active noise cancellation). The signal generator used is the Keysight 33210A (Keysight Technologies, Santa Rosa, California), and the oscilloscope used is the Keysight MSOX3024T (Keysight Technologies, Santa

Rosa, California). All time-domain data is acquired through the embedded system, transmitted via USB, and stored on a MacBook (Apple Inc., Cupertino, California).

Two basic verifications are conducted: gain and frequency response evaluations. Namely, the gain should be sufficient to amplify typical EEG signals (5-300 μV) and the passband should include 0.5 to 150 Hz [9]. The gain is estimated by first using a high value gain resistor (100kΩ) to reduce the gain of the overall circuit. Then the resistor value is sequentially reduced in 8 steps to 680Ω to achieve higher gain. Lastly, the gain at normal operation, which requires exceedingly low input amplitude to test directly, is extrapolated from the obtained values. The frequency response is obtained by sweeping a 30 mV peak-to-peak test signal from 0.01 Hz to 10 kHz.

A set of differential-mode and common-mode recordings is obtained for two channels at three signal generator output frequencies: 1 Hz, 10 Hz, and 100 Hz at 20 mV peak-to-peak. From now on, the positive input pin of the instrumentation amplifier will be referred to as the input pin, and the negative input will be referred to as the reference pin. In the differential-mode setup, the reference pin is connected to ground, and the input pin is connected to a signal generator. In the common-mode setup, both the reference pin and the input pin are connected to the same signal generator. In each setup, 20 seconds of each frequency are acquired. The common-mode rejection ratio (CMRR) formula is simplified from equation 6 to equation 7 because the input amplitudes are identical. CMRR is calculated with a Fast Fourier Transform (FFT) of the entire segment of data. The signal-to-noise ratio (SNR) is calculated with a zero-mean Welch's method with 4096-point FFT segments and a 1024-point overlap. The resulting power spectral density series is then integrated according to equation 8 to compute the SNR.

$$CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}}) \quad (3)$$

$$CMRR(dB) = 20 \times log_{10}(\frac{Vout_{differential}}{Vout_{common}}) \quad (4)$$

$$SNR(dB) = 10 \times log_{10}(\frac{P_{signal}}{P_{noise}}) \quad (5)$$

The DRL testing setup is the same as the differential mode setup, with an additional connection from the DRL output to ground. An active soldering iron is brought close to the input pin to simulate 60 Hz noise. Then, 20 seconds of time series data is acquired with the DRL enabled compared to disabled.

B. Evoked Potential Acquisition

Three 3M Red Dot 2238 electrodes (3M Company, Maplewood, Minnesota) are attached to a participant to acquire blinking artifact. One electrode is placed between the fp1 and fp2 positions according to the 10-20 international standard. The reference electrode is placed on the left mastoid, and the ground electrode is placed on the right mastoid. The evoked potentials are then recorded when blinking or eye movements occur.

C. Embedded System Interrupt Timing Verification

S0 on GPIO pin 6 naturally switches between low (0 V) and high power (3.3 V) every time the interrupt timer is called to control the first bit of the MUX selector. This gives a convenient measurement of how long between interrupts are actually taking place, since adding any additional code to measure timing accuracy may affect the timing. By plugging GPIO 6 to a DSO-X 2024A (Keysight Technologies, Santa Rosa, California) oscilloscope, the time between state changes was read. To do this, the horizontal zoom was set such that only 1 cycle was shown, then the preview was paused and resumed randomly to measure the time difference between states. For the given parameters of 10 channels at 1kHz, this function should be called at 10 kHz or 100 μs between state changes. Timings longer than this are sampling too infrequently and timings lower than this are sampling faster than optimal.

D. Circuit Case Drop Testing

To ensure the circuit case provides adequate protection from accidental drops the following testing was completed: Using an unpopulated circuit board screwed into a case, drop the case 8 times each from 3 different heights. Starting at 0.75m, randomize the drop order between flat on the base, flat on top, flat on front face, flat on back face, flat on left side, flat on right side, one top front edge and one corner. Then move on to randomizing the same orientations at 1m and then a third time at 1.2m onto a hard surface. Between drops visually inspect the case, including the circuit board by taking the cap off for any signs of cosmetic or functional damage. Record and categorize the damage from every drop, cosmetic damage is defined as any normal use of the case and circuitry will not be impaired, e.g., scratches, dents or similar damage. Functional damage is defined as any damage that impairs the use of the product in some way, like permanent damage to the circuit board or extensive damage to the case such that a port is not accessible or the circuit board no longer fits. The case will be considered successful if it can survive the above drops with only cosmetic damage and can still function.

IV. RESULTS

A. Electrical Circuit

The completed fabricated circuit is populated for system verification. The total component cost is $42 and the PCB costs $7. A detailed breakdown of the cost is available in Appendix G. The two leading costs for the circuit are the instrumentation amplifiers and the decoupling capacitors.

The observed gain is 11% ±2.1% lower than the theoretical values. The passband range for the bandpass filter is observed to be 0.1Hz to 200 Hz. The average center for the level shifter is 1.60 V ±0.06 V while the theoretical value is 1.65 V (Figure 7B). The observed values and the design parameters are summarized in Table 2.

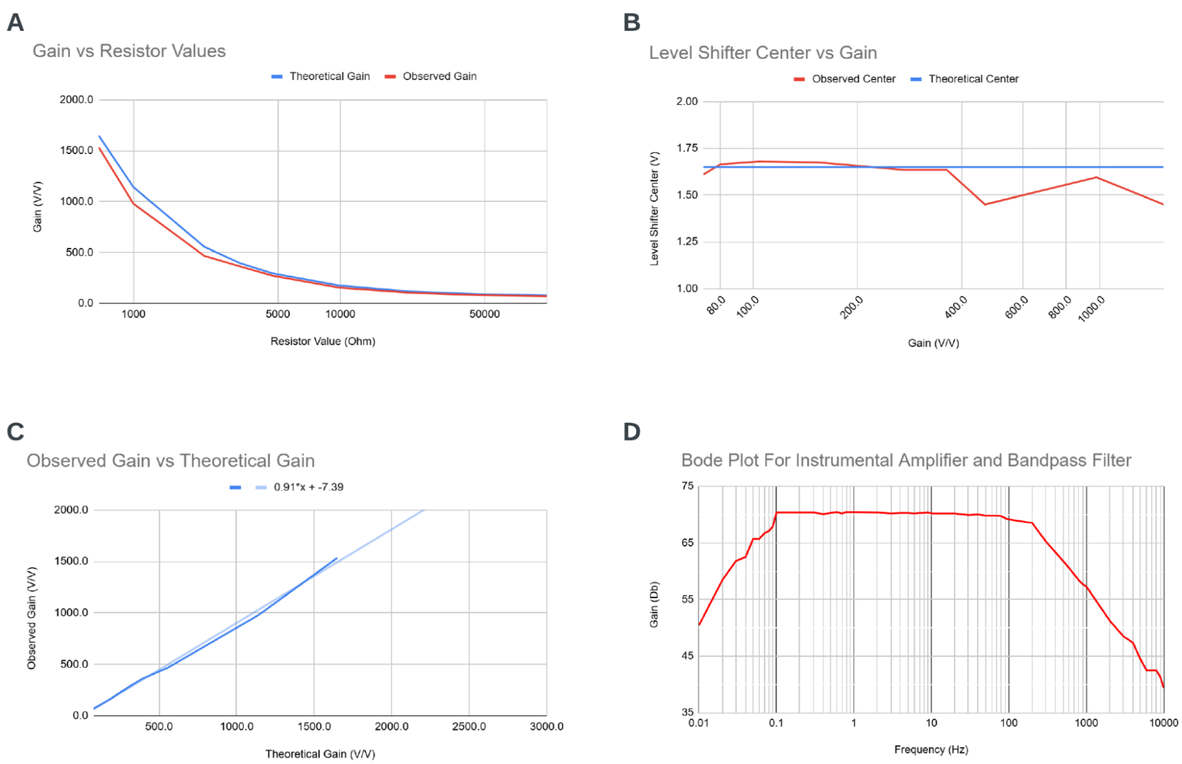

Figure 7: Manual Test Results for the Analog Front End. A. Gain vs Resistor values plot for the analog front end. B. Level shifter center vs gain plot. C. Observed vs theoretical gain plot with the linearly regressed projection. D. Bode plot of the frequency response for the populated third channel within the parallel series configuration. Note that the overall gain occurs at 50.47 dB, which is 333 V/V, and the passband frequency extends from .1Hz to 200 Hz.

Table 2: Design Requirements Evaluation

Category	Design Requirement Value	Observed Value
Passband Range	0.1 to 150 Hz	0.1 to 200 Hz
Gain	2757 V/V	2501 V/V
Level Shifter Center	1.65V	1.6±0.06V

Cost	$100	$61

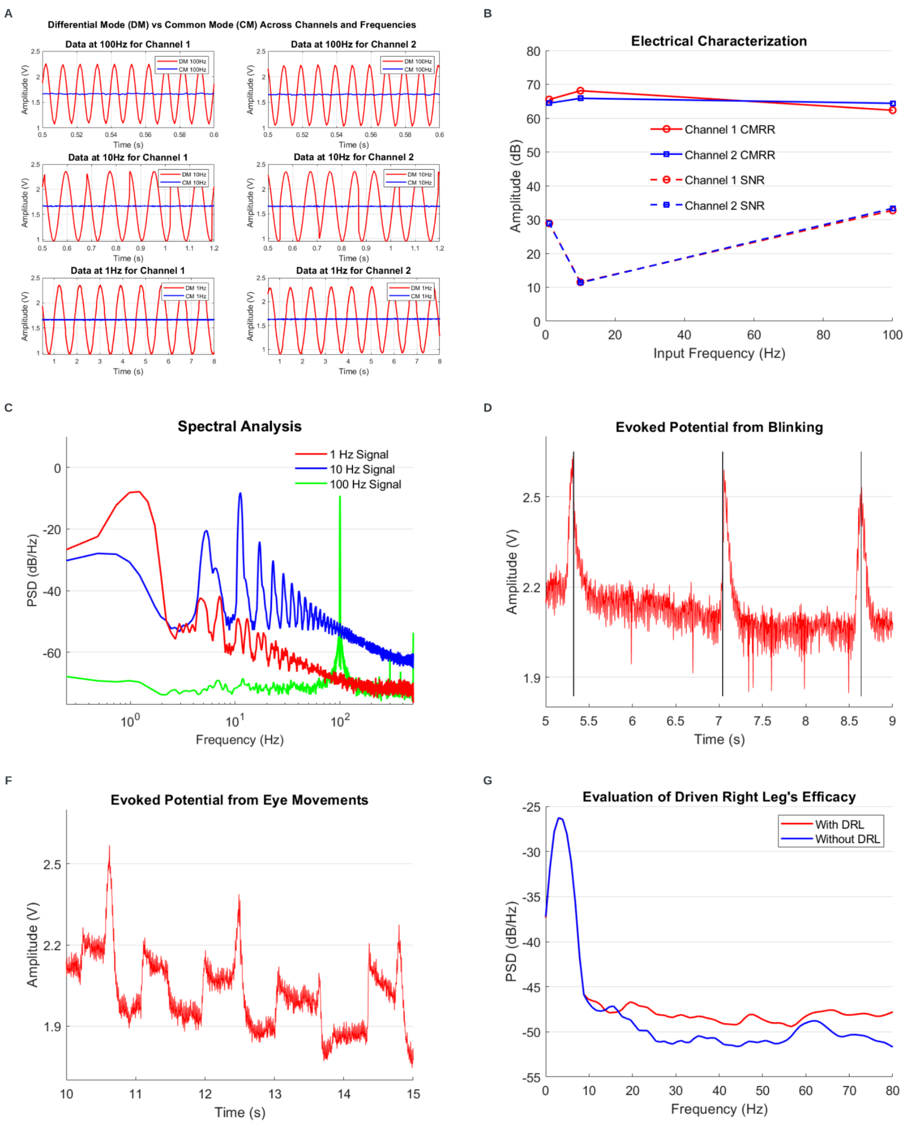

Figure 8: Electrical Characterization of the analog front end. A. Example time series acquired in the differential-mode and common-mode setups. Two channels are tested with three input frequencies: 1 Hz, 10 Hz, and 100 Hz. B. CMRR and SNR for the two channels plotted against input frequency. C. Spectral analysis of the differential-mode data. D. Recorded evoked potentials from blinking. F. Recorded evoked potentials from blinking and eye movements. G. Spectral analysis of the signal acquired with and without DRL engaged. Input frequency is set at 1 Hz.

Representative time series data is plotted in Figure 8.A. The mean CMRR is 65.1 dB with a standard deviation of 1.92 dB (Figure 8.B). The minimum, 62.3 dB, is observed at 1 Hz input frequency, and the maximum, 68.1 dB, is observed at 10 Hz input frequency. The mean SNR is 24.5 dB with a standard deviation of 10.3 dB (Figure 8.B). The minimum, 11.3 dB, is observed at 10 Hz input frequency, and the maximum, 33.3 dB, is observed at 100 Hz input frequency. The notable decrease in SNR at 10 Hz can be further illustrated in Figure 8.C, where the noise amplitude rolled off more slowly at 10 Hz compared to 1 and 100 Hz.

The evoked potential from blinking can be observed at the marked positions in Figure 8. D. Changes to steady state voltage due to eye movements, in addition to blinking, can be observed in Figure 8.E. While this setup is intended to record EEG signal, it is reasonable to assume that a substantial component can be attributed to Electromyogram (EMG) signals.

From spectral analysis, the DRL did not alter the power spectral density of the signal and increased the power spectral density of noise from -48.8 dB/Hz to -47.9 dB/Hz.

B. Ear Clip

The results from the ear clip comfort testing showed the effectiveness of the design. At the start, all participants rated the ear clip comfort as “Extremely Light” on the discomfort scale or an average of 7.25. At the end of the test, the team did see a 34.5% increase in the mean comfort level of the participants. An increase from 7.25 value to 9.75 was recorded (Figure 9). Throughout the test, some mechanical failures were encountered in the ear clip design itself. The clip started to show signs of permanent deformation. Another observation from the data was that the participants with attached earlobes had an increase in mean discomfort level of 1.5 for the initial and final surveys. This information shows that comfort is negligible for the current ear clip design. Moving forward, the team will focus on revising the ear clip design to create more durability. Further testing will be completed to test the durability of our new design.

Table 3: Summary of the Discomfort Evaluation of the Ear Clips

Subject #	Comfort Level After 10 Seconds	Comfort Level After 10 Minutes
1	8	11
2	8	10
3	7	8
4	6	10

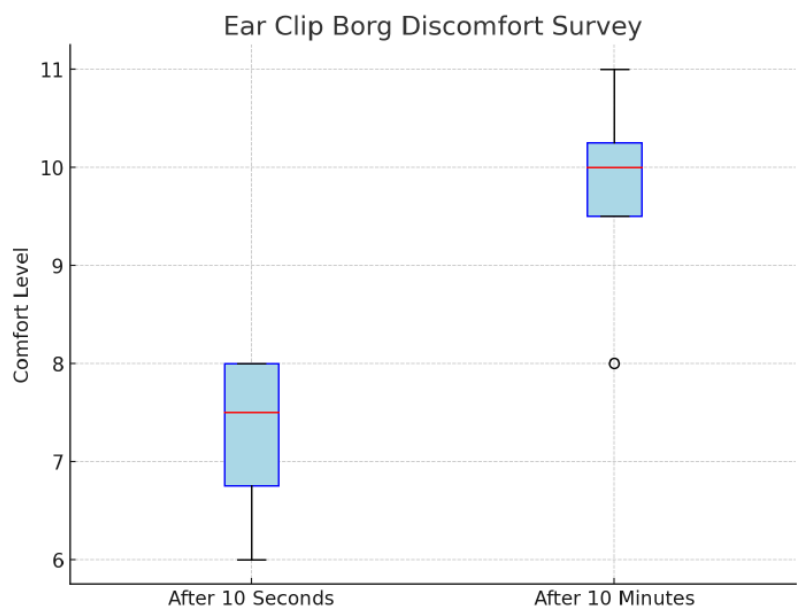

Figure 9: Box Plot Summary of the Borg Discomfort Survey for Two Participants

The ear clip comfort testing was conducted to assess the level of comfort a patient experiences during brief exposures to ear clip pressure. The team aimed to understand the amount of pressure exerted on a patient. According to a study involving ICU patients, a pressure of 2759 Pascals sustained overnight can lead to symptoms of pressure ulcers [17]. The team sought to determine whether the ear clip would exceed this threshold. To investigate this, the team employed a test using a pressure-sensitive resistor, which was attached to the tip of the ear clip. Literature indicates that thick earlobes typically range from 7 to 8 mm [18]. To simulate various earlobe thicknesses, the team used different quantities of paper, creating values ranging from 4 to 10 mm (Figure 10). Resistance readings were taken using a multimeter and then converted to pressure values using the calibration curve provided. The test results, shown in Figure 11, indicate that at a maximum earlobe thickness of 10 mm, the pressure applied by the ear clip peaked at 2000 Pascals—well below the 2759 Pascal threshold of concern.

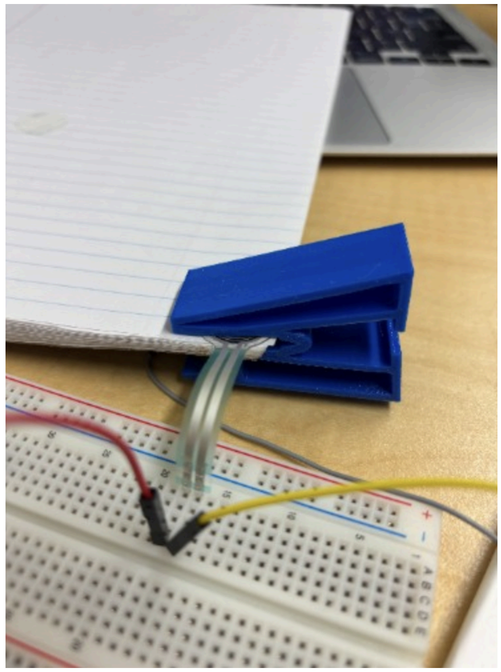

Figure 10: Force Testing Set Up

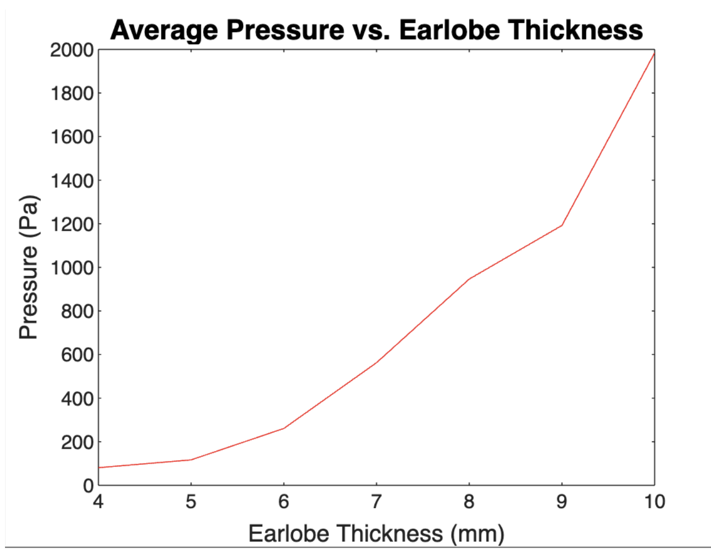

Figure 11: Ear Clip Pressure vs Earlobe Thickness

C. Embedded System Interrupt Timing Results

Over 20 samples read the timing between interrupts was found to be on average 100.18 ± 0.24 µs standard deviation, or 9.82 ± 0.02 kHz for the interrupt function, leading to an overall sampling rate of 0.98 kHz (Figure 12). This was about 2% away from the desired sampling frequency of 1 kHz. Future work could be considered to see if artificially raising the interrupt sampling rate value by about 2% could bring the actual sampling rate closer to the desired value. Figure 12 below shows the difference in µs between 100 and each sample. Some samples were right on the expected timing while others were up to 0.62 µs after expected.

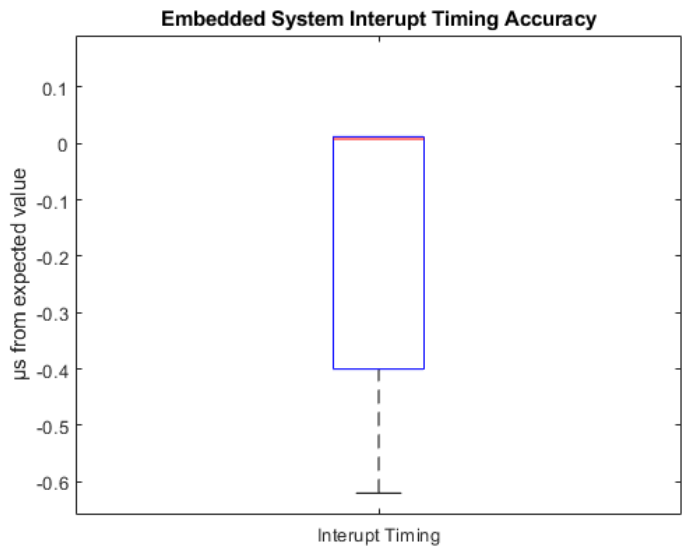

Figure 12: Embedded System Interrupt Timing Accuracy.

D. Circuit Case Drop Testing Results

The case survived with only minor cosmetic damage from drop testing from 3 heights. In all three heights about half the time no damage was observed, the other times there was minor damage like the lid popping off which could be easily placed back in and rarely was found with a scratch, screws coming out or damage to one of the clips that hold the lid on. Damage to lid grips may have been made worse by having to take off the lid to inspect the circuit board for damage, something that should not be common for normal use. Drop testing order and resulting damage at 0.75, 1 and 1.2 meters are listed below in tables 4-6.

Table 4: Case Drop Testing Results 0.75 m.

Orientation	Damage
Flat on base	None
Flat on right side	1 screw fell out
Flat on left side	None
Flat on back face	Last 2 screws fell out
Flat on front face	None
Flat on top	Rough scratches on edges
One top front edge	None
One corner	None

Table 5: Case Drop Testing Results 1 m.

Orientation	Damage
Flat on front face	None
Flat on back face	None
Flat on right side	Lid came off

Flat on base	Lid came off
One top front edge	None
One corner	Lid came off, lid grip broke
Flat on left side	Lid came off
Flat on top	Lid came off

Table 6: Case Drop Testing Results 1.2 m.

Orientation	Damage
Flat on top	Lid came off
One corner	None
Flat on back face	None
One top front edge	None
Flat on base	Lid came off
Flat on left side	None
Flat on front face	Lid came off
Flat on right side	Lid came off

V. DISCUSSION

A. Testing Results

Upon testing, it was determined that the gain range of 3,053 V/V to 95,563 V/V was sufficient for amplifying low-amplitude signals (5 µV) and avoiding saturation of higher amplitude signals (300 µV). Variation allowed by the potentiometer permits easy adjustment to circuit gain to individualize signal acquisition on every EEG. For the level shifter, the slight variation in the averaging center can be easily compensated by a variable gain resistor. Acquiring a passband range of 0.1-200 Hz is acceptable as it includes the 0.1-150Hz design constraint while remaining under the Nyquist frequency of 500 Hz. The CMRR achieved is highly satisfactory for this design, particularly given the low cost constraint. The results of the DRL remain inconclusive about the effectiveness of decreasing the noise. Further data would need to be acquired to determine if there is any statistical significance.

B. Gain Inaccuracies

The gain inaccuracies can be at least partially explained by resistor inaccuracies (5%). Assuming 5% deviation, a maximum deviation of +8.11 V/V to -8.96 V/V can be observed at the output of the instrumentation amplifier, +2.83 V/V to -2.56 V/V at the output of the bandpass filter, and +0.05 V/V to -0.05 V/V at the output of the level shifter. Taken together, a maximum reduction to an overall gain of 2015 V/V is possible due to resistors. Thus, our observed value can be well explained by resistor inaccuracies alone. Additionally, the intent of this circuit is to visualize EEG signals; the precision of the gain does not affect this. With the variable gain amplifier provided by the potentiometer, all signals within the target range should be acquired without clipping.

C. Hardware Remarks

The current design of the PCB features potentiometers which are rotated at a 90 degree angle. These components should be substituted to feature components which sit vertically. This will allow for the design to fit more securely within the case, as well as improve ease of use. In order to accomplish this, the footprints for the potentiometer will need to be adjusted slightly. When utilizing this PCB, all channels of the design should be populated, regardless of how many are employed. If all channels are not populated, there is a large increase in noise and final outputs can become skewed. This is likely due to floating endpoints within the circuitry.

D. GUI

The GUI included within this design is a unique addition when compared to other systems. It allows the user to directly see the output from their own computer, without the use of expensive software or complicated coding. The ease of use contributes to the accessibility of this project, especially for under-resourced areas.

E. Head Cap and Ear Clip

Although performance testing of the fabric EEG head cap was not completed, the design successfully demonstrated adaptability by accommodating a wider range of head sizes compared to previous iterations. This improvement addresses a key limitation in earlier designs and enhances overall usability. Additionally, the ear clip design was evaluated for comfort using both quantitative and qualitative methods. The Borg discomfort survey provided subjective feedback, while pressure measurements offered objective data, confirming that the clip remained within a safe pressure range. These findings support the potential for improved user comfort in future applications.

E. Patient Usage

This board was developed to acquire EEG signals from the brain. Testing to date has focused exclusively on verifying the board's electrical performance, rather than evaluating it in a medical or clinical setting. Consequently, additional testing is required prior to using the device on patients. However, the system has been designed with patient use in mind, and is prepared for clinical employment following validation on patient populations.

VI. CONCLUSION

In this work, we propose the design of an open source 10 channel EEG headcap that can sample at 1 kHz with a 12 bit resolution for under $100. The team developed a head cap, ear clips, protective case, embedded system, GUI, and the analog front end PCB. The ear clips were found to be comfortable among participants, with an initial average Borg score of 7.25 and a 10-minute score of 9.75. The system achieves an average CMRR of 65.1 dB and SNR of 24.5 dB. While the active noise cancelling fails to increase recording performance, evoked biopential from blinking can still be distinctively captured. The GUI can display all ten channels in real time with configurable parameters. The embedded system timing achieves a standard deviation of 0.24 μs in the sampling period. The protective case suffered no significant damages during drop testing.

VII. ACKNOWLEDGEMENTS

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IX. APPENDIX

Appendix A: Product Design Specifications

<u>Function</u>

Epilepsy is a common chronic neurological disease characterized by abiding recurrent seizures [1]. The most recent WHO report cites 50 million people affected worldwide, whose risk of premature death is up to three times that of the general population [2]. Electroencephalogram (EEG) is the most widely used detection and analysis procedure for epilepsy, which records cortical electrical activity. Identifying EEG patterns and seizure foci is critical for the diagnosis of specific epilepsy syndromes and, consequently, the selection of appropriate therapy [3]. However, 80% of epilepsy patients live in low- and middle-income countries, the majority of which do not have access to EEG systems or treatments [2]. Therefore, affordable EEG systems that can be rapidly and broadly deployed are in critical need.

<u>Client requirements</u>

- A single-channel sampling rate of at least 1 kHz.
- 12- to 16-bit analog-to-digital converter resolution.
- Periodic reading of electrode impedance to detect improper electrode contact.
- Total system cost at or below $100.
- 10-channel analog frontend.
- Driven by wall-plugged power supply.

Design requirements

Physical and Operational Characteristics

<u>Performance requirements</u>

The devices will be used for 20 to 40 minutes per patient per procedure [4]. The frequency of usage is dependent on the medical facility.

<u>Safety</u>

The device must be sanitized between uses, and the skin contact electrodes must be replaced. Since the device involves prolonged skin contact, irritation, discomfort, and allergic reactions are possible. The device consists of active electrical components and wires; thus, it must be carefully handled and not be tampered with while powered on. Furthermore, the device's temperature during operation must not exceed 40 ℃.

<u>Accuracy and Reliability</u>

The system should have a sampling rate of at least 1 kHz per client's requirement. The analog-to-digital converter (ADC) should encode with at least a 12-bit resolution to capture finer details of the EEG waveform. Low impedance, e.g., 5 k**Ω** electrodes, should be used to enhance signal clarity. To improve ease of use, the device should detect improperly connected electrodes. Additionally, signal filtering is required to reduce capacitive coupling effects from power lines and electromyogram interference.

Typically, the reliability of a diagnostic system is measured by its positive predictive value; however, the accuracy of epilepsy classification is critically dependent on monitoring duration and is unrealistic to calculate within the scope of this project [5].

Life in Service

The system must remain operational for 3-4 years with proper daily usage, ensuring durability and consistent performance. It should function effectively within a temperature range of 0-40°C without any drop-off in EEG signal amplitude, as higher temperatures are observed to negatively affect signal quality in existing EEG systems [6]. Additionally, the system must be easy to clean between uses, as it will be exposed to various cleaning products. The head cap should remain functional for 3-4 years with daily cleaning.

Shelf Life

The product should maintain its integrity and functionality in storage for at least ten years at room temperature. It must withstand transportation without any wear or damage and be designed to endure harsh conditions during transit. The product should tolerate storage temperatures ranging from -20°C to 100°C, as it may encounter extreme environments during transportation.

Operating Environment

The EEG cap must ensure consistent and secure contact between the electrodes and the scalp to accurately capture brain signals while maintaining user comfort over extended periods. The materials should be soft, lightweight, and non-invasive, providing a secure yet non-irritating fit. The EEG system should also function reliably in various temperatures typical of indoor and controlled outdoor environments, e.g., 0-40°C. The cap and circuit board should resist sweat, moisture, and mild physical impacts, ensuring long-term durability and accurate signal collection.

Ergonomics

The system should be accurate and fit users with a maximum horizontal head circumference between 50 to 64 cm, similar to other commercially available EEG electrode caps [7, 8]. The system should be effective for users of any hair volume and texture between bald and hair type 1 to 4d [9].

Figure 1. *Examples of hair types*

Size

The entire system should be portable and easy to carry. The cap and electrodes should be able to fit on most children and adults.

Weight

The system should weigh less than 1 lb and cause no neck strain while wearing.

Materials

There are no printed circuit board (PCB) materials restrictions as the device is not intended to operate in extreme environments. Operating temperatures, coefficient of thermal expansion, and electrical characteristics are non-critical factors. Dry electrodes are preferred, typically composed of conductive silicone or gold-plated electrodes, as requested by the client [10]. The head cap should resist cleaning solutions, e.g., ethyl or isopropyl alcohol and chlorine-releasing agents.

Aesthetics, Appearance, and Finish

The cap's design will ensure the patient feels comfortable in the environment. All wires should be as enclosed as the system allows. The circuit board will have a cover to shield the view from the patient. The appearance will be sleek and neutral to avoid any strong aversions. The appearance of the electrodes and the board will be professional in portraying the device's safety.

Production Characteristics

Quantity

One unit is needed for the scope of this project. This unit should be created to be reproducible on a large scale.

Target Product Cost

For one unit, the entire system costs at or below $100.

Miscellaneous

Standards and Specifications

The Code of Federal Regulations Title 21, Volume 8 Chapter 1 Part 882: Neurological Devices provides specific standards concerning electroencephalograms (EEGs) and other commercially distributed neurological devices intended for humans. Sec. 882.1400 states that EEGs are used to measure and record the brain's electrical activity and are classified as a class II medical device [11]. This means they have to follow general regulatory control and special controls, including performance standards, special labeling requirements, and post-market surveillance [12]. They must also go through the 510(k), a premarket submission process that proves the device is similar to one currently operating and showcases that it is safe [13]. To be considered within this classification, the EEG can have recording hardware, monitor, and basic software; however, this does not include electrodes, a complex software analysis system (to either auto-detect or analyze events), or a system with more than 16 electrodes. Additionally, this device is not allowed to be used in sleep studies. EEG electrode/lead tester is a device used to test the impedance of electrodes. It is classified as a Class I device, along with an EEG signal spectrum analyzer and an EEG test signal generator. Cutaneous electrodes are applied directly to the skin to record or apply electrical stimulation and are classified as a Class II medical device.

In addition to FDA standards, IEEE recommended practice for EEG Neurofeedback Systems details practices that should be abided by [14]. The system must adhere to the IEC 60601-1 Safety and Essential Performance standard to follow safety procedures. The EEG should be sold as a medical device, where the user is trained to operate the equipment properly. System software shall be available to allow all parts of the system to be analyzed as needed. This includes electrodes, which should have an expected lifetime, performance, polarization rate, and long-term stability. Cleaning techniques, application, and impedance checking should accompany these electrodes. Several different specifications should be included for the primary component, as listed in Table 1.

Along with these documents, several ISO and IEC standards are applicable. IEC standard 80601-2-26:2019 details the particular requirements for EEGs' basic safety and performance [15]. ISO standard 22077-5:2021 specifies the format of waveforms created during EEG to support one recording session [16].

***Table II**: Specifications that must be listed, as stated by IEEE Recommended Practice for EEG [14]*

Amplifier Specifications	Frequency specifications	Analog to Digital Conversion
Input impedance	Magnitude response	Number of bits, number of channels, and type input/output channel
DC/AC coupling (time constant if ac coupled)	Phase response	Sampling rate
Noise/sensitivity (RMS and/or peak-peak voltage, given bandwidth or application, noise spectrum)	Corner frequency / frequencies	Anti-aliasing filter specification
Signal input range	Decay and rolloff	Resolution, quantization error, and/or least-sig bit size (eg performance over temperature, hysteresis, etc.)
Signal output range	Decibel (dB) attenuation in stopband	ADC technique
Ground type (active/not) or direct reference line noise		Channel-to-channel isolation and digital channel
CMRR		
Gain		
Bandwidth		
Supply voltage/current consumption		
Impedance checking specifications (stimulus, measurement time/duration, absolute accuracy, relative accuracy)		
Amplification		

<u>Customer</u>

The device is tailored for medical clinics in underdeveloped areas; thus, its cost and durability are prioritized. Borth criteria are detailed in this document above. Additionally, the device should be intuitive to use and include detailed instructions in various languages.

Patient-related concerns

Four main patient-related concerns will be addressed:

- **Patient Comfort & Skin Irritation**: Long-term EEG monitoring may cause discomfort or skin irritation, especially due to the electrodes' contact with the scalp. Proper cap design, skin preparation, and using hypoallergenic materials are essential to reduce discomfort and prevent rashes or sores.
- **Movement Restrictions**: Patients must remain relatively still during EEG recording to avoid artifacts from muscle movements. This can be challenging, especially for pediatric or uncooperative patients, leading to inaccurate readings.

- **Infection Risk & Hygiene**: Reusing EEG caps and electrodes poses a risk of infection if they are not properly sanitized between uses. Ensuring strict hygiene protocols and using disposable components when necessary can mitigate this risk.
- **Psychological Stress or Anxiety** Some patients, particularly children or those with certain neurological conditions, may experience anxiety or discomfort during the EEG process due to unfamiliar equipment or the need to remain still for extended periods. Clear communication and a calming environment can help alleviate these concerns.

Competition

Most EEG systems are intended for medical use and are inaccessible to consumers and medical facilities in underdeveloped countries. Although consumer EEG systems with relatively low costs exist, none of the multi-channel systems cost close to the $100 threshold (Table III). Commercialized products like Neurosky, Muse, and Emotiv often feature non-essential Bluetooth functionalities and auxiliary sensors that contribute to their cost. Their channel count and sampling rate also fall short of the client's requirements. Open EEG's modular EEG system offers the most competitive pricing for its performance. However, its ATmega8 employs a 10-bit ADC with six channels that fail to meet the performance requirements.

Table III*: Summary of Existing Consumer EEG Devices*

Product	Channel Count	Sampling Rate (Hz)	Bit Depth	Wireless	Cost (USD)
Neurosky MindWave	1	512	12	Yes	130
Muse2	4	256	12	Yes	300
Emotiv MN8	2	128	14	Yes	400
Emotiv Insight	5	128	16	Yes	500
Emotiv EPOC X	14	256	14-16	Yes	1000
Emotiv Flex Saline	32	256	16	Yes	2000
Open BCI Complete Kit	16	125	24	No	2500
Open EEG	2-6	Up to 15.4k	10	No	200-400

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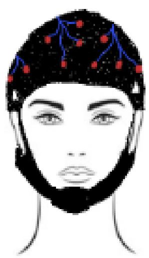
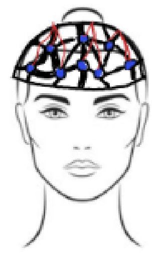
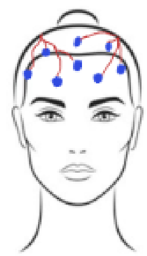
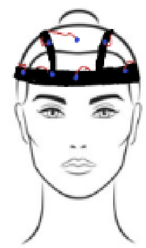
Appendix B

Table IV: Head Cap Design Matrix

	Store Bought		3D Print		No Head Cap		DIY		
									
	Points out of 5	**Weighted Score**							**Weight**
Cost	0	0	4	80	5	100	4	80	**20**
Safety	5	75	4	60	3	45	3	45	**15**
Accuracy	5	70	4	56	1	14	2	28	**14**
Repeatability	4	56	5	70	1	14	2	28	**14**
Ease of Use	5	65	4	52	2	26	2	26	**13**
Durability	5	60	3	36	4	48	2	24	**12**
Comfort	5	35	4	28	4	28	3	21	**7**
Ease of fabrication	5	25	2	10	5	25	3	15	**5**
Total		**386**		**392**		**300**		**267**	**100**

Cost:

The expected cost to produce one electrode cap. Store Bought is by far the most expensive, with most models being well over $100, No Head Cap requires no additional material so is therefore the cheapest. DIY and 3D Print have the potential to be inexpensive depending on material choice, but do have some cost associated with them.

Safety:

All electrode caps should be safe for use and provide stable electrode connection, while none of these designs provide major risk, Store Bought was most safe since it provides the most protection between the electrodes and head while other designs may be at higher risk for electrodes to come loose.

Accuracy:

The electrode cap design must keep each electrode accurately at the associated biological marker. Store bought was ranked the most accurate since with more material covering the head, strain to cause electrode drift to incorrect locations is minimized by more material. No head cap is the least accurate since it requires

the Doctor to place electrodes manually before each test.
Repeatability:

The design must be able to be constructed and run repeatedly with no dip in performance of the product. The environment, patient, and the person running the test are all factors that could change. Despite these changes, the results should remain consistently accurate. The 3D printed design was ranked the highest because the team would have control over the production of each component unlike the store bought. The no head cap and DIY both ranked lower as these have a much higher chance of human error leading to less accurate results over multiple trials.
Ease of Use:

Ease of use refers to the difficulty for the tester to run the test on the patient. This product needs to be fairly easy to use so that a trained operator can consistently give the test and the patient has no issues during the test. The store bought design ranked highest because the commercial products are tailored to the interest of the consumer, giving it a good chance to be easy to use. The DIY and no head cap ranked lowest as these would require a lot more training on how to create/execute the test.

Durability:

This design must be durable in order to withstand travel, repeated use, and movement as the patient adjusts the product in order to fit the cap to their head. The store bought design was ranked the highest as since these are commercially available, the quality of the product will most likely be higher than our other design ideas. The no head cap scored higher on this metric as there is not much that could be damaged to the product itself. While the DIY and 3D printed designs have a higher chance of human error as well as a design tailored to performance and not durability.

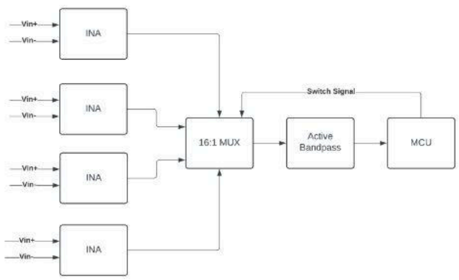
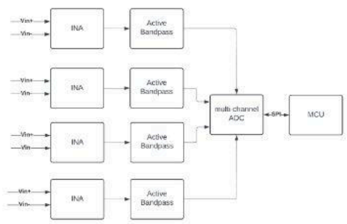
Comfort:

The design must be comfortable enough for the patient to get through the test without any difficulties but the team decided this was not of top priority due to the importance of other factors. The store bought design ranked the highest amongst this metric as since those are typically more expensive the company creating the design has put more effort into the comfort of the product than our other designs. The DIY ranked the lowest as this design would be very simplistic and tailored towards accomplishing the task of running the test accurately without a focus on comfort.

Ease of fabrication:

Ease of fabrication was not weighted as highly as other factors due to most of these products being easy to assemble. The 3D printed design ranks the lowest as this would be the most difficult to fabricate due to the size and structure of the cap itself. The store bought would be easily fabricated as there would be no assembly, the cap would arrive fabricated.

Table V: Analog Front End Design Matrix

			
	Single-channel ADC + MUX	**Multi-channel ADC**	**Weights**
Cost	26	16	26
Accuracy	16	21	26
Ease of fabrication	20	15	25
Firmware Complexity	5	3	5
Components Availability	14	10	17
Sum	**81**	**65**	100

Cost:

Cost is defined as the listed price of the component on Digikey. The cost for creating the single-channel ADC + MUX costs less to produce, as the multi-channel ADC costs significantly more than the single channel ADC.

Accuracy:

Accuracy is defined as the amount of noise contributed by the individual component. There are less components in the multi-channel ADC, so there is less probability of noise being created. However, neither circuit was given a 5, as the components will generate some amount of noise. This will particularly be true due to the low cost objective; more noise will likely enter the signal acquisition as a result of using cheaper components.

Ease of fabrication:

Ease of fabrication is defined as the amount of time and effort that it takes for the team to fully assemble the system, e.g., soldering, PCB designs. The multi-channel ADC has less individual components, so it will be easier to fabricate.

Firmware Complexity:

Firmware complexity is defined as the associated coding and wiring complexity. The multi-channel ADC received a higher score because of the ease of coding. Creating the code to alternate through each electrode channel is more difficult that reading all of the separate signals at once.

Component Availability:

Components availability is defined as the number of equivalent components available on Digikey. Equivalency refers to the ability of the component being swapped without changes to other components. There are more equivalent swaps for the creation of the single channel circuit, so it was given a higher rating.

Appendix C Head Cap Testing Data

Table VI: Raw Data from Head Cap Landmark Alignment

Subject 1								Subject 2							
% distance from nasion landmark to inion	Measured Distance (cm)	Expected Distance (cm)	Difference	Percent Error	Mean absolute Percent Error	Median absolute percent error	Standard Deviation	% distance from nasion landmark to inion	Measured Distance (cm)	Expected Distance (cm)	Difference	Percent Error	Mean absolute Percent Error	Median absolute percent error	Standard Deviation
10%	3.5	3.8	-0.3	-7.89	5.80	5.26	2.00	10%	5.5	3.9	1.6	41.03	7.29	1.71	13.2
20%	7	7.6	-0.6	-7.89				20%	8	7.8	0.2	2.56			
30%	11	11.4	-0.4	-3.51				30%	12.5	11.7	0.8	6.84			
40%	14.5	15.2	-0.7	-4.61				40%	15.5	15.6	-0.1	-0.64			
50%	18	19	-1	-5.26				50%	19.5	19.5	0	0.00			
60%	22	22.8	-0.8	-3.51				60%	23	23.4	-0.4	-1.71			
70%	29	26.6	2.4	9.02				70%	27	27.3	-0.3	-1.10			
80%	32	30.4	1.6	5.26				80%	31	31.2	-0.2	-0.64			
90%	36	34.2	1.8	5.26				90%	39	35.1	3.9	11.11			

Appendix D: PSRR Testing Protocol

PSRR = 20 log (Δvin/Δvout)

Materials

1. AC+DC network summing device
2. Oscilloscope (ideally one that can automate frequency sweep)

Protocol

1. Connect 5V DC to the summing device and an AC 60 Hz source with 100mV PtP
2. Connect the recording electrode and reference to 1V DC
3. Observe the PtP ripple amplitude at Vout
4. calculate PSRR

Appendix E: CMRR Testing Protocol

Stage 1 - Testing without Mux

1. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.

2. Hook up the input of the first instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes of the first instrumental amplifier.

3. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.

4. Apply a 20Hz 100 μV sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 μV sine wave to the wave generator that is attached to both the input and reference input.

5. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.

6. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.

7. Perform calculations using the equation $CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}})$, where the $G_{differential}$ is the value of the output at 20Hz, and G_{common} is the value of the output at 60Hz. Both the $G_{differential}$ and G_{common} should be expressed in voltage.

8. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.

9. Repeat this protocol with 5Hz, 10Hz, 15Hz, 25Hz, and 30Hz all replacing the 20 Hz signal, keeping the signal amplitude at 100 μV.

Stage 2 - Testing with Mux

10. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.

11. Hook up the input of the instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes. All of the inputs for the instrumental amplifier should receive the same signal, as should all of the reference nodes.

12. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.

13. Apply a 20Hz 100 μV sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 μV sine wave to the wave generator that is attached to both the input and reference input.

14. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.

15. Inspect the data and note anything of significance that could account from the addition of the mux. This can include spikes or lapses in data.

16. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.

17. Perform calculations using the equation $CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}})$, where the $G_{differential}$ is the value of the output at 20Hz, and G_{common} is the value of the output at 60Hz. Both the $G_{differential}$ and G_{common} should be expressed in voltage.

18. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.

19. Repeat this protocol with 5Hz and then 30Hz replacing the 20 Hz signal, keeping the signal amplitude at 100 μV.

Appendix F: Commercial EEG Comparison

Material

- Tucker-Davies Technology recording cart
- EEG testing board
- 5-6 gold cup electrodes
- electrode gel/cream
- abrasive gel/paper towel
- tape measure
- marker
- gauze

TDT setup

- The recording and reference electrodes are attached to the TDT amplifier
- recording software is opened and ready to record

PCB setup

- The EEG PCB board should be connected to a computer via a micro USB cable.
- The recording, reference, and DRL electrodes are attached to the board.
- Appropriate recording software/terminal is opened and ready to record

Procedure

1. Identify attachment location according to the 10/20 standard.
    1. Use a tape measure to drape across the head to coincide with the sagittal plane.
    2. Make sure the tape measure begins at the nasion and ends at the inion.
    3. Mark the skin at 10% of the length from the nasion (Fp1).
2. Clean the skin at the location and use abrasive gel or paper towel to reduce impedance.
3. Apply electrode gel to the gauze.
4. Apply adequate electrode gel to the cup electrode and place the stem of the electrode on the gelled gauze

5. Press gently on the skin
    1. repeat for the two recording electrodes and others
6. begin recording
7. end recording after 5 mins
8. align recordings
9. adjust for sampling frequency if there is any difference
10. calculate dB error
    1. 20log(ground truth/PCB)
11. calculate variance and mean

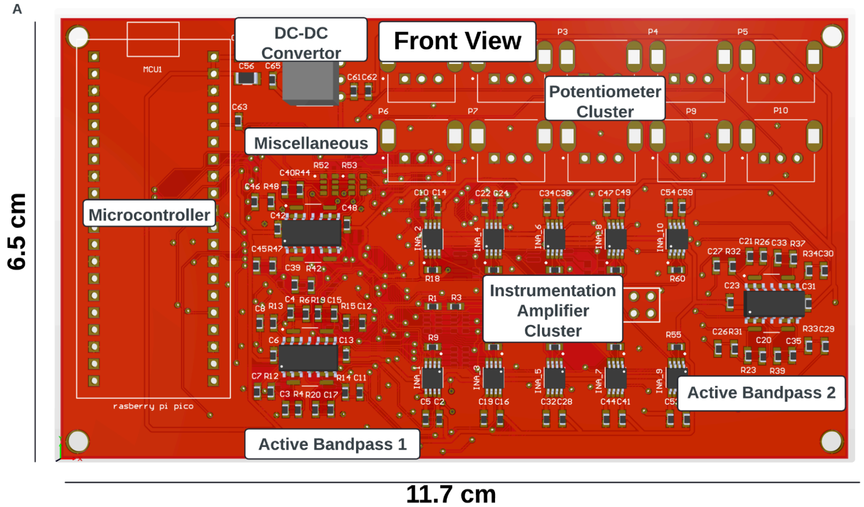
Appendix G

Table VII: Electronics Cost

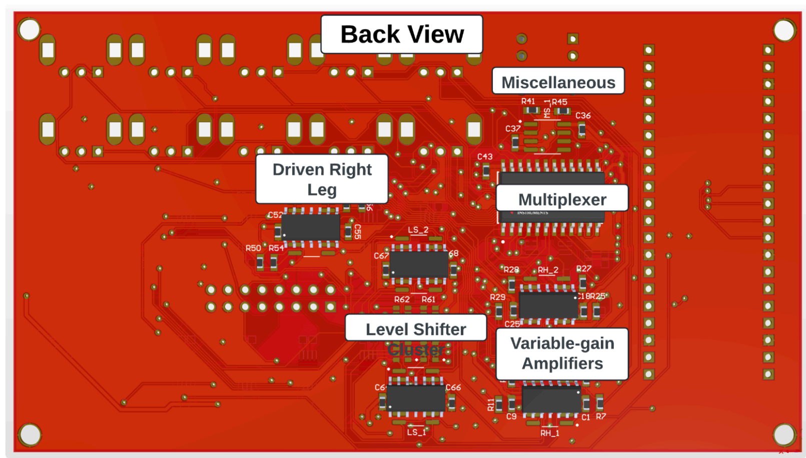
Component	Manufacturer	Manufacturer Part#	Cost Each	QTY	Total
Instrumentation Amplifier	Texas Instrument	INA827AIDGKR	1.906	10	19.06
Multiplexer	Texas Instrument	CD74HC4067M96	0.57	1	0.57
Microcontroller	Rasberry Pi	RP2040	4	1	4
Operational Amplifier	Texas Instrument	TLV9004IDR	0.408	8	3.264
Operational Amplifier	Texas Instrument	TL072CDR	0.26	1	0.26
Male Header	Samtec	HTSW-108-07-G-D	0.9	1	0.9
.1uF capacitor	Samsung Electro-Mechanics	CL10B104KA8NNNC	0.004	55	0.22
10uF capacitor	Samsung Electro-Mechanics	CAP CER 10UF 10V X5R 0603	0.032	9	0.288
100uF cappacitor	Samsung Electro-Mechanics	CL31A107MQHNNNE	0.52	1	0.52
220pF capacitor	Samsung Electro-Mechanics	CAP CER 220PF 50V X7R 0603	0.027	6	0.162
DC-DC convertor	TC962EPA	TC962EPA-ND	4.09	1	4.09
10K Resistor	Stackpole Electronics Inc	RAVF164DJT10K0	0.022	2	0.044
20K Resistor	Stackpole Electronics Inc	RAVF164DJT20K0	0.03	2	0.06
390K Resistor	Stackpole Electronics Inc	RMCF0603FT390K	0.02	4	0.08
160K Resistor	Stackpole Electronics Inc	RMCF0603FT160K	0.02	6	0.12
470 Resistor	Stackpole Electronics Inc	RMCF0603JT470R	0.019	6	0.114
1K Resistor	Stackpole Electronics Inc	RMCF0603FT1K00	0.02	2	0.04
360 Resistor	Stackpole Electronics Inc	RMCF0603FT360R	0.02	8	0.16
180 Resistor	Stackpole Electronics Inc	RMCF0603JT180R	0.019	4	0.076
4.3M Resistor	Stackpole Electronics Inc	RMCF0603FT4M30	0.024	6	0.144
10K potentiometer	Same Sky (Formerly CUI Devices)	PT01-B120D-B103	0.758	10	7.58
				Total	41.752

Appendix H: PCB Layout

A



B



Appendix I: PCB specifications

Table I: Manufacturing Parameters of the PCB

Parameter	Value
Size (mm)	135.8×114.3
Thickness (mm)	1.6
Minimum Hole Size (mm)	0.3
Material	FR-4 TG 150-160
Layers	2
Via Process	Tenting Vias
Finished Copper (oz)	1
Surface Finish	Hot Air Solder Leveling with Lead
Minimum Track Width (mil)	6
Minimum Track Spacing (mil)	6

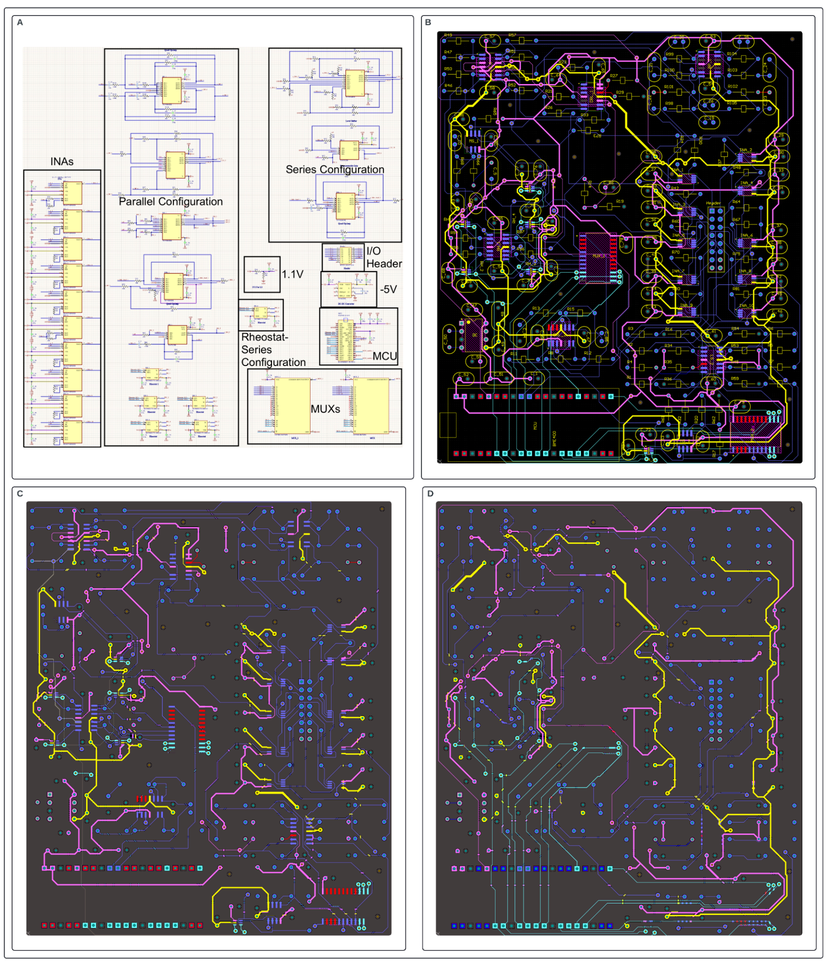


Figure 7: Final Design of the PCB. A. Final schematic diagram of the PCB. B. Front side of the PCB without polygon fills. VCC and VEE are colored pink and yellow, respectively. Analog signals are colored purple, and digital signals are colored cyan. C. Front side of the PCB with polygon fills and hidden silkscreen. The ground signal is colored grey. D. Backside of the PCB with polygon fills and hidden silkscreen.