Affordable Diagnostic EEG System for Viral-induced Epilepsy

Richard Yang[1,2], Ellie Dingel[1], Mark Rice[1] and Elliott Harris[1]

[1]Department of Biomedical Engineering, University of Wisconsin-Madison, Madison WI 53701 USA

[2]Department of Computer Sciences, University of Wisconsin-Madison, Madison WI 53701 USA

***Abstract*-Epilepsy is a prevalent neurological disorder affecting approximately 50 million people worldwide, with 80% of cases occurring in low- and middle-income countries where access to diagnostic tools like electroencephalograms (EEGs) is limited. Conventional EEG devices are prohibitively expensive, restricting early diagnosis and treatment planning. This study presents the development of an affordable, portable, and reliable 10-channel EEG system for diagnosing viral-induced epilepsy, with a targeted production cost of under $100. The system comprises a custom-designed printed circuit board (PCB) for signal acquisition and amplification, a 3D-printed head cap for electrode placement, and an embedded system for real-time signal processing and data transmission. The analog front-end utilizes a Raspberry Pi RP2040 microcontroller, an instrumentation amplifier, and a multiplexer-based architecture to enhance signal fidelity while minimizing switching artifacts. Two circuit configurations—parallel and series—were evaluated to optimize performance and cost-effectiveness. Initial testing demonstrated a frequency response of 0.1 Hz to 200 Hz, sufficient gain amplification for low-amplitude EEG signals, and accurate electrode placement with a 5.8% to 7.3% mean absolute error in landmark alignment. However, challenges such as mechanical deformation of the ear clip and inconsistencies in the common-mode rejection ratio (CMRR) necessitate further hardware refinements. Future work will focus on refining the head cap design for broader fitment, improving ear clip durability, and optimizing the analog circuitry for enhanced signal quality. This low-cost EEG system has the potential to significantly improve epilepsy diagnostics in resource-limited settings, enabling earlier intervention and better patient outcomes.**

I. INTRODUCTION

It is estimated that 1 in 26 Americans develops Epilepsy at some point in their lifetime. Epilepsy is a neurological disorder that causes sporadic seizures affecting 50 million people worldwide[1]. Various treatments exist for Epilepsy, such as anti-seizure medications (AEDs), ketogenic diets, seizure-preventing devices, and even surgery[2]. However, diagnosis of the sub-type of Epilepsy is required before a treatment plan can be devised. The primary way to detect Epilepsy without observing recurring seizures is through an electroencephalogram (EEG)[3]. The EEG system is placed on the patient's scalp and is used to detect the electrical impulses in the human brain. Currently, EEG devices are expensive and difficult to obtain. Medical-grade EEG systems cost tens of thousands of dollars, and open-source projects are still prohibitively expensive. OpenBCI, a partially open-source project known for its brain-computer interface devices, offers an eight-channel biosensing board, EEG cap, and electrodes for $2,578[4]. Although this device may be effective, areas without the necessary resources could not afford a stock of these devices to detect and diagnose epilepsy. 80% of epilepsy patients live in low- and middle-income countries, the majority of whom have access to treatment but not diagnostic equipment[5]. This project aims to create a reliable, accurate, and inexpensive EEG device. The product must receive, process, and display signals from ten channels in a format that a medical professional can easily interpret.

Electroencephalogram (EEG) signals originate from the synchronized electrical activity of pyramidal neurons in the cerebral cortex[6]. When neurons communicate, they generate postsynaptic potentials—small voltage changes that occur when neurotransmitters bind to receptors on the neuronal membrane. These potentials propagate through neural tissue via volume conduction and combine to form electrical fields that can be measured at the scalp. Individual action potentials are too brief (1-2 ms) to be detected by scalp electrodes; instead, EEG primarily captures the summation of slower postsynaptic potentials (10-250 ms) from thousands to millions of neurons firing in synchrony [6]. The amplitude of these signals is quite small, typically ranging from 5 to 300 microvolts when measured at the scalp, necessitating significant amplification for clinical interpretation. Different frequency patterns in these signals correspond to various brain states and neurological conditions, making EEG valuable for diagnosing disorders like epilepsy [6].

Epilepsy is a brain disorder characterized by abnormal neuron activity, leading to misfires in the brain and resulting in seizures. Two or more of these seizures, with an unknown cause, is what is called Epilepsy. Anyone at any age can develop Epilepsy. However, it is most common in early childhood or old age [1]. Conventionally, EEG uses scalp electrodes that record a

variety of active neuronal potential fluctuations. The potentials are aggregations of neuronal action potentials [6]. These recordings usually range from 0.5 to 100 Hz and their amplitudes ranges from 5 μV to 300 μV [6]. An example EEG of absence seizure is shown in Figure 1 and is characterized by a behavioral arresting with concurrent 3-Hz wave discharges [7]. EEG can detect miscommunications between neurons. These channels that detect those miscommunications will tell the physician that the patient may have epilepsy. Using more channels across different brain regions can give a higher chance of detecting these disruptions in brain activity. One study found that Epilepsy affects the hippocampus, amygdala, frontal cortex, temporal cortex, and olfactory cortex most often. However, disruptive activity can be detected across many brain regions [8]. This justifies the constraint of 10 channels rather than eight or fewer channels, giving a higher chance of detection.

Neurodiagnostic tests like EEG are challenging to perform in less fortunate areas. A study completed by the American Academy of Neurology says that in most low-income countries surveyed during the study, only the top 10% or 20% of the population could afford tests below catastrophic levels. In surveyed lower-middle-income countries, >40% of the population, on average, could not afford neurodiagnostic tests [3]. This is in stark contrast to high-income countries like the United States, and Western Pacific World Health Organization regions, where more than 70% of the total population can afford EEG tests [3]. Dr. Brandon Coventry, a postdoctoral fellow in the Department of Neurosurgery at the University of Wisconsin School of Medicine and Public Health, decided to create this project to find a way to solve this problem. For the device to be useful for less fortunate areas, Dr. Coventry aims to keep the production cost under 100 dollars. This device must also be compatible with various head shapes and sizes. The team found that the 50-64 cm circumference range would capture all regular occurring head sizes [9]. The device must remain in operation for 3-4 years without a dip in performance. The device must be able to be transported, stored, and implemented in a variety of temperatures depending on the environment. Please see Appendix A for the team's complete product design specifications for this product.

Figure 1: Example EEG of Absence Seizures [7]

This project also includes the processing of low-amplitude signals from the brain. This consists of filtering and amplifying the signal. The design must be cost-effective and easy to fabricate. Filtering 60 Hz powerline noise is vital in any environment where capacitive coupling from the powerline and other electrical interferences exist. One commonly used filtering technique is a bandpass filter, which uses a circuit of varying electrical components to achieve a calculated sampling frequency. Instrumentation amplifiers are critical elements extensively used for input buffering and high voltage gain [10].

II. SYSTEM DESIGN

The system consists of three components, the electrical circuit for obtaining the signal, the embedded system for digitizing the system and imbuing interactive elements, and the EEG headcap for ease of operation. A comprehensive specification of the system, including codes and standards, can be found in Appendix A.

A. Electrical Circuit

a). Circuit Design

The electrical circuit acquires, amplifies, and processes ten EEG channels. The frequencie ranges of interests are delta (0.5 to 4 Hz), theta (4 to 7 Hz), alpha (8 to 12 Hz), beta (16 to 31 Hz), and gamma (36 to 90 Hz)[11]. The sampling frequency is 1 kHz per channel.

Two configurations, parallel and series, are developed in Altium Designer (Altium, San Diego) to satisfy the above requirements. Other designs considered can be found in Appendix B. The goal of parallel configuration is to minimize switching artifacts, while the series configuration aims to reduce the number of components, consequently reducing cost. To compare the operational characteristics of the two configurations, five of each channel are printed on a PCB (PCBWay, Shenzhen, China) for testing. Each channel of the parallel configuration has a dedicated instrumentation amplifier, bandpass filter, level shifter, and variable gain amplifier (Figure 2A). All the channels then terminate at the MUX and are read directly by the ADC. Since each channel is independent from one another, they are ready to be sampled at any given time, and the only switching artifact produced is from the MUX itself. On the other hand, the series configuration only has a dedicated instrumentation amplifier and level shifter for each channel (Figure 2C). Thus, on every switching event, the signal has to be stabilized not only across the MUX but also across the bandpass filter and the variable gain stage.

The schematic diagram of a single channel of both configurations is shown in Figures 2B, 5D. Both bandpass filters are tuned to corner frequencies 0.1 Hz and 168 Hz with Equation 1. LT1920 is used as a general-purpose instrumentation amplifier, and a fixed 10 kΩ resistor replaces the rheostat. For convenience, the MUX is modeled as a short.

$$f_c = \frac{1}{2\pi RC} \tag{1}$$

The gain of the INA is given by Equation 2 and the gain of the programmable amplifier is given by Equation 3. The gain for both level shifters is 0.5 V/V. For the parallel configuration, the bandpass filter has a gain of 26.9 V/V, while the series configuration has a gain of 27.9 V/V. Thus, the total gains of the parallel and series configurations are given by Equations 4 and 5, respectively. Importantly, for the series configuration, all the amplifiers have to be non-inverting since the level shifter must be placed first in front of the MUX. Therefore, if inverting amplifier topology is used, the positive DC shift induced by the level shifter will become negative.

$$5 + \frac{80k\Omega}{R_G} \tag{2}$$

$$\frac{R_{Rheo}}{470} + 1 \tag{3}$$

$$2757 \times \left(\frac{R_{Rheo}}{470} + 1\right) \tag{4}$$

$$2857 \times \left(\frac{R_{Rheo}}{470} + 1\right) \tag{5}$$

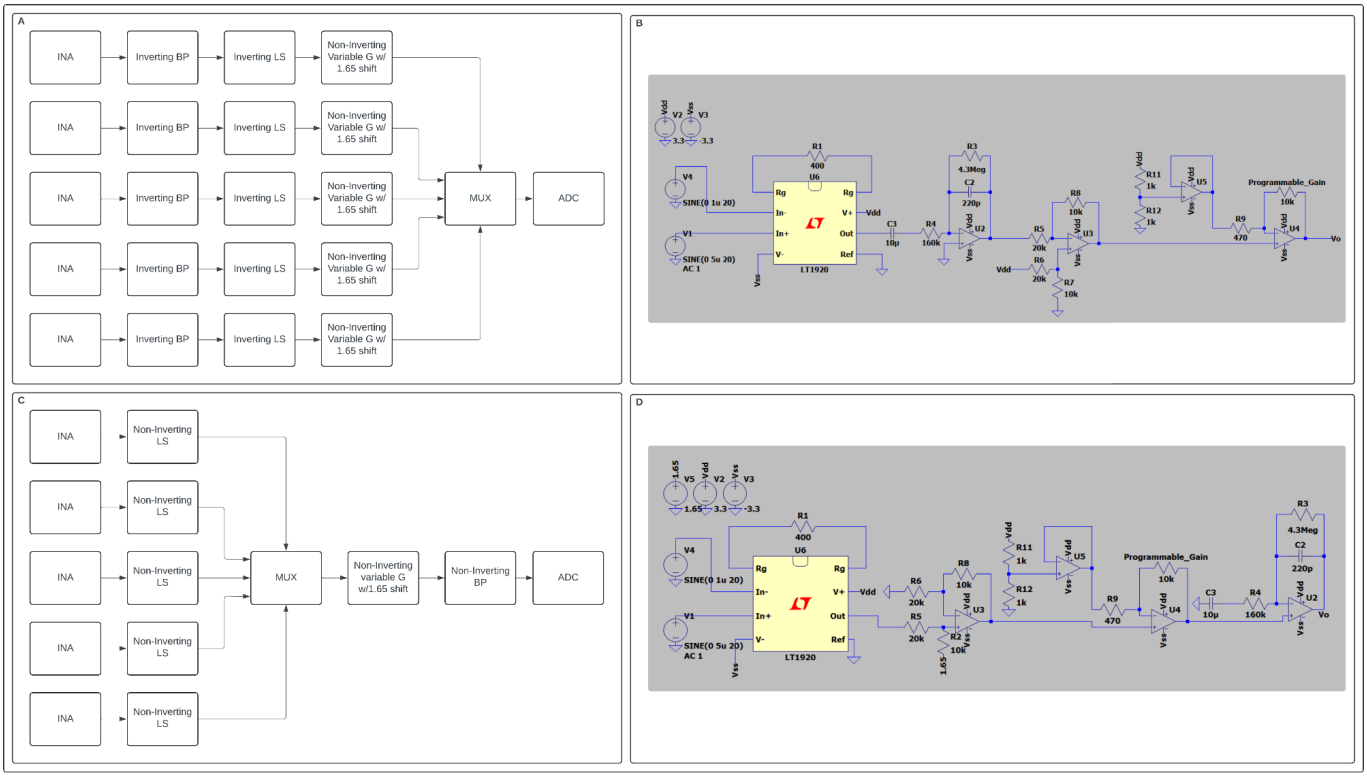

Figure 2: Circuit design. A. Block diagram of the parallel configuration. B.Schematic diagram of a single channel of the parallel configuration. C. Block diagram of the series configuration. D. Schematic diagram of a single channel of the series configuration.

The heart of the analog front end is the Raspberry Pi RP2040 (Raspberry Pi Foundation, Cambridge, England) in the Raspberry Pi Pico package. It features three on-board ADCs, each samples with 12-bit resolution at 500 ksps, exceeding the 10 ksps minimum requirement (Appendix A). The VBUS pin of the RP2040 is connected directly to the VCC pin of the micro USB, which powers the MCU and the entire analog front end. A microchip TC962EPA (Microchip Technology, Chandler, Arizona) is then used to create VEE. The INA827AIDGKR (Texas Instrument, Dallas, Texas) is used as the instrumentation amplifier since it provides ±40 V input protection, a satisfactory slew rate of 1.5V/µs, and enough -3db Bandwidth of 600 kHz. The multiplexer is the CD74HC4067M96 (Texas Instrument, Dallas, Texas), which allows for the sampling of all signals at a 1kHz rate. The general operational amplifiers consist of TLV9004IDR and TL072CDR (Texas Instrument, Dallas, Texas), which provide four circuits and two circuits, respectively. MCP40D17T-104E/LT digital rheostat (Microchip Technology, Chandler, Arizona) can be programmed to be up to 100kΩ and is coupled with a general operating amplifier to form a variable gain amplifier. Additionally, 100 nF, 10 µF, and 100 µF capacitors are used throughout the PCB as decoupling capacitors. Finally, various resistors, capacitors, and headers complete the circuit.

The schematics and PCB routing of the two configurations are completed in Altium Designer (Altium, San Diego, California). The final schematic is shown in Figure 3. Five channels of each configuration are developed, all terminating at a common RP2040 MCU. The first channel of each configuration is tied to a driven right leg circuit for active noise cancellation. The parallel configuration is populated with four quad operational amplifiers, a dual operation amplifier, and five rheostats. The serial configuration consists of two quad operational amplifiers, a dual operation amplifier, and one rheostat.

The components of the PCB are then placed and routed. Signal traces are 0.2 mm wide to minimize crosstalk, and the spacing between traces is as wide as possible. Power traces are 0.5 mm wide to provide low resistance and routed as short as possible. Analog traces are primarily on the front side of the PCB, while digital traces are primarily on the back side of the PCB to minimize digital interference with analog signals. Lastly, the front and back sides are filled with ground with stitching vias distributed in void spaces. The PCB is then printed through PCBWay (PCBWay, Shenzhen, China) with parameters specified by Appendix H.

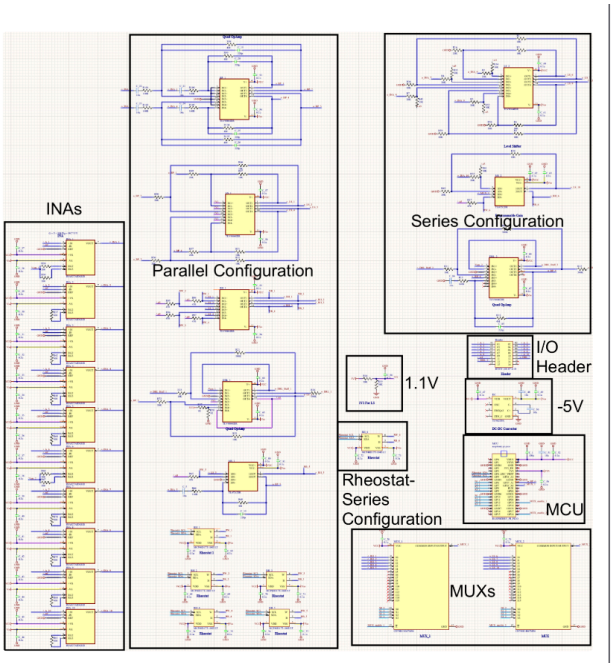

Figure 3: Final schematic diagram of the PCB.

b). Circuit Verification

Two main preliminary verifications are conducted: gain and frequency response evaluations. The precision of the two parameters is of lesser importance than the assessment that the observed values are sufficient for operation. Namely, the gain should be sufficient to amplify typical EEG signals (5-300 μV) and the passband should include 0.5 to 150 Hz [6]. The tests are only conducted on a single channel of the parallel configuration as the embedded system is not yet fully developed to test the serial configuration.

The gain is estimated by first using a high value gain resistor (100kΩ) to reduce the gain of the overall circuit. Then the resistor value is sequentially reduced in 8 steps to 680Ω to achieve higher gain. Lastly, the gain at normal operation, which requires exceedingly low input amplitude to test directly, is extrapolated from the obtained values.

The frequency response is obtained by sweeping a 30 mV peak-to-peak test signal from 0.01 Hz to 10 kHz.

B. Head Cap and Ear Clip

The head cap is 3D printed with 20 grams of thermoplastic polyurethane (TPU) and 40 grams of support material. The final prototype was printed using Bambu Lab TPU 95A HF with a diameter of 1.75mm +/- 0.003 mm. TPU gives a cost-effective, flexible feeling ideal for putting on and removing the head cap. A flexible material allows stretching and moving of the head cap for slight variations in head size. TPU costs about four cents per gram and is commonly used in 3-D printing, while other flexible, commonly used materials like soft PLA may cost about twelve cents per gram, or flexible uncommon materials like TPS cost around eight cents per gram.

The first design of the ear clip would utilize a torsional spring and 2 grams of polylactic acid (PLA) 3D printed material. The spring utilized was a 45 degree 1.5mm wire diameter spring. The team was able to locate this spring in the biomedical engineering lab free of charge. However, due to fabrication difficulties, the team decided to pivot from this design. The current ear clip design is also 3D printed using approximately 1 gram of polylactic acid (PLA).

The head cap model is generated using the Neurocaptian plugin for Blender [12]. See Appendix C for detailed instructions. Neurocaptain converted computed tomography (CT) scans to a brain mesh and, eventually, a head cap model. Importantly, a preconfigured version of Blender must be downloaded for Windows 11, and Octave, a scientific and mathematical-focused programming language, must be added to the path. The final prototype was created using the provided “20-24 year” brain mesh, 4x4 circular holes, and 4.00 thickness.

After this, post-processing in SolidWorks is done to reduce necessary support material. Splitting the model about halfway up the head cap and then creating a spline through the intersected points can create a half-circle edge to later reattach the model after printing. This reduces the necessary support material since the top middle of the head cap does not need to be supported while the bottom outer portion is printed.

The Final prototype was printed using a BambuLab A1 3-D printer using 0.4 mm layer height, 0.62 mm line width, two wall loops, 15% infill density, 500 mm/s travel speed, tree supports at a 30 degree threshold and 360 degree celsius nozzle temperature. This model was sliced in Bambu Studio.

The team originally researched an existing ear clip design that could be purchased and utilized. However, the currently available lowest-cost EEG ear clip cost approximately 15 dollars. This price would not meet the product design specifications. The preliminary and final prototype were designed using SolidWorks. The preliminary design was created at an angle of 36 degrees to allow for compression of the torsional spring to create tension. The final design utilized the elasticity of the PLA material so when the ear clip is pinched, the clip would return to its original shape and pinch the earlobe. An eight millimeter hole was created on one side of the clip in order to house the electrode.

The final prototype (Figure 4A) of the 3D printed headcap based on the “20-24 yr” brain mesh, is printed from TPU. The final prototype of the 3D printed ear clip is shown in Figure 4B.

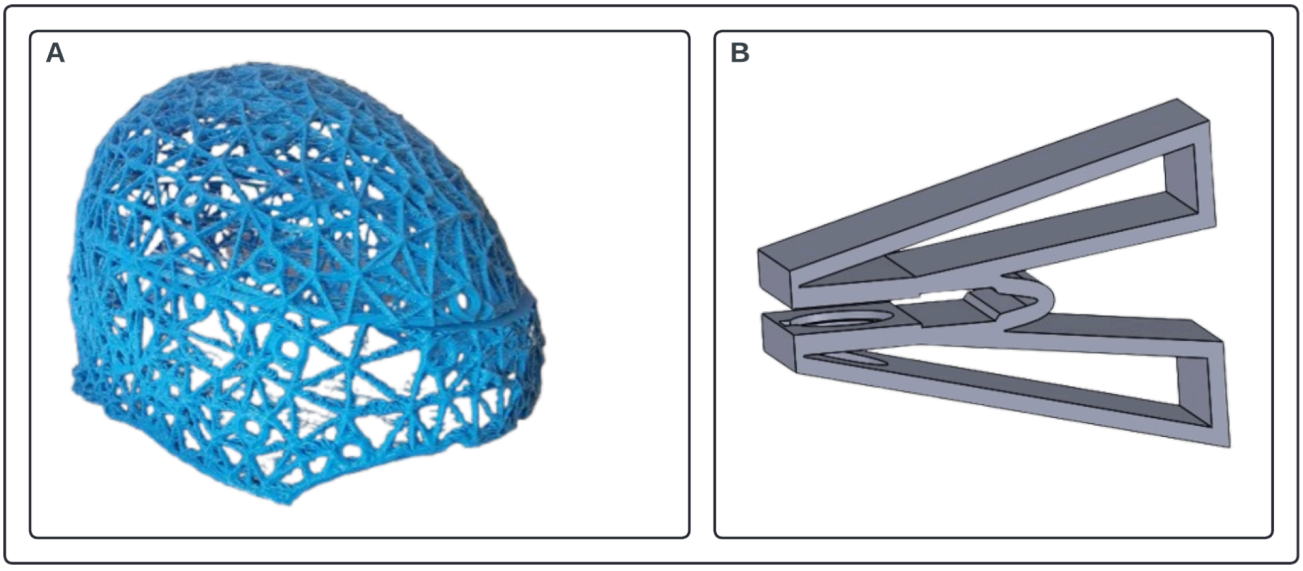

Figure 4: Headcap prototypes. A. Final Prototype of 3D Printed Headcap. B. Final Prototype of 3D Printed Ear Clip

C. Embedded Systems

The Embedded system is intended to control on board electronics, read analog signals and digitally send those signals over USB. It must be written in a way to accommodate up to 10 channels, sample each channel at 1 kHz and run on the RP2040. The RP2040 will connect with and control the CD74HC4067M96, and read the output from that, as well as changing the resistance of the MCP40D17T-104E/LT over I^2C. Using the C programming language, programmed within Visual Studio Code using the Raspberry Pi Pico pluggin the embedded system will first, initialize GPIO and I^2C pins, set an interrupt function at the number of channels multiplied by 1 kHz sample rate and set baseline resistance for MCP40D17 changing R_{Rheo} in Equations 3 - 5. After this, inside the interrupt function, the embedded system will first read the analog signal from the output of the CD74HC4067M96, assign it to its appropriate channel and then cycle through to switch the CD74HC4067M96 to the next channel. It is done in this order to ensure that the CD74HC4067M96 has sufficient time to switch the output channel before trying to read the analog output from that channel. Once all channels have been read from, the embedded system will send the voltage from each channel over USB to an external PC for further analysis and GUI interaction and recording.

III. RESULTS

A. Electrical Circuit

The fabricated PCB is shown in Figure 5, which is partially populated for system verification. The total component cost is $54 and the PCB costs $7. A detailed breakdown of the cost is available in Appendix G. The two leading costs for the circuit are the instrumentation amplifiers and the decoupling capacitors.

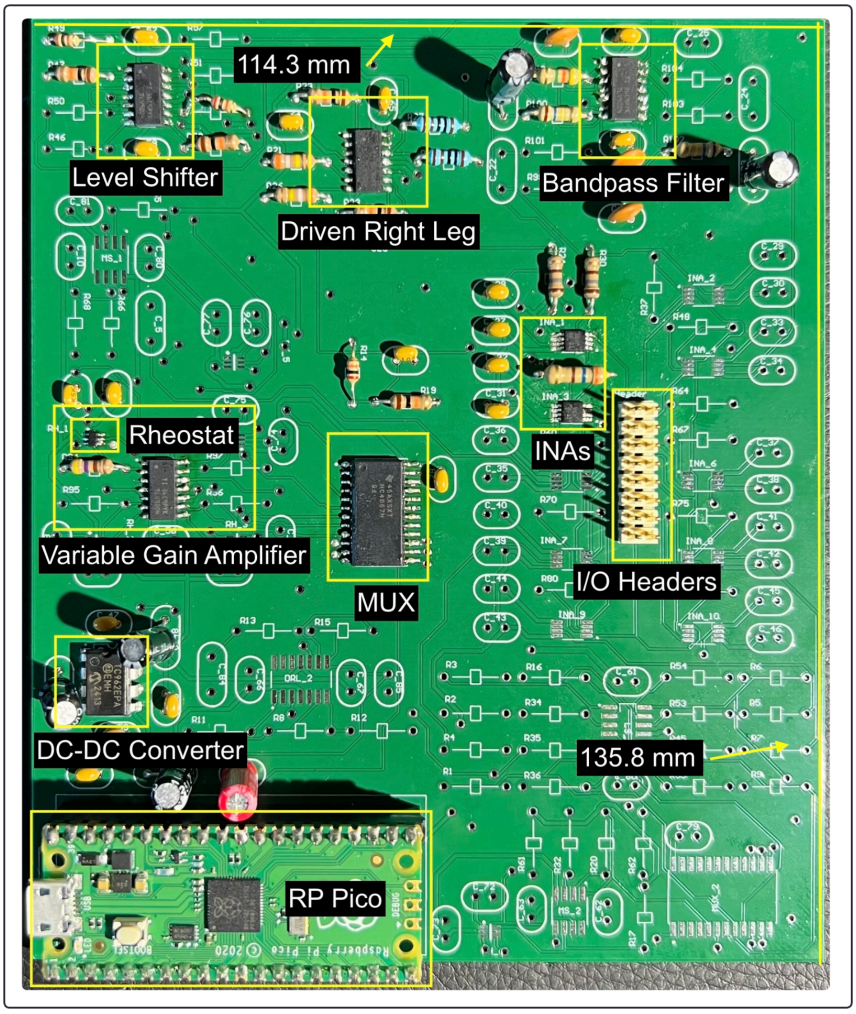

Figure 5: Final Prototype of the Analog Front End

a). Preliminary Evaluation

The observed gain is 11% ±2.1% lower than the theoretical values. The projected gain at the operation is 2501 V/V while the theoretical value is 2757 V/V for the parallel configuration (Figure 6A,C). This is sufficient for amplifying low-amplitude signals (5 µV) and avoids saturating higher amplitude signals (300 µV). The average center for the level shifter is 1.60 V ±0.06 V while the theoretical value is 1.65 V (Figure 6B). This is a negligible difference as 0.05 V can be easily compensated by the variable gain amplifier.

The passband range is observed to be 0.1 Hz to 200 Hz, which is acceptable as it includes the 0.1 Hz to 150 Hz design constraint (Figure 6D).

The observed values and the design parameters are summarized in Table I.

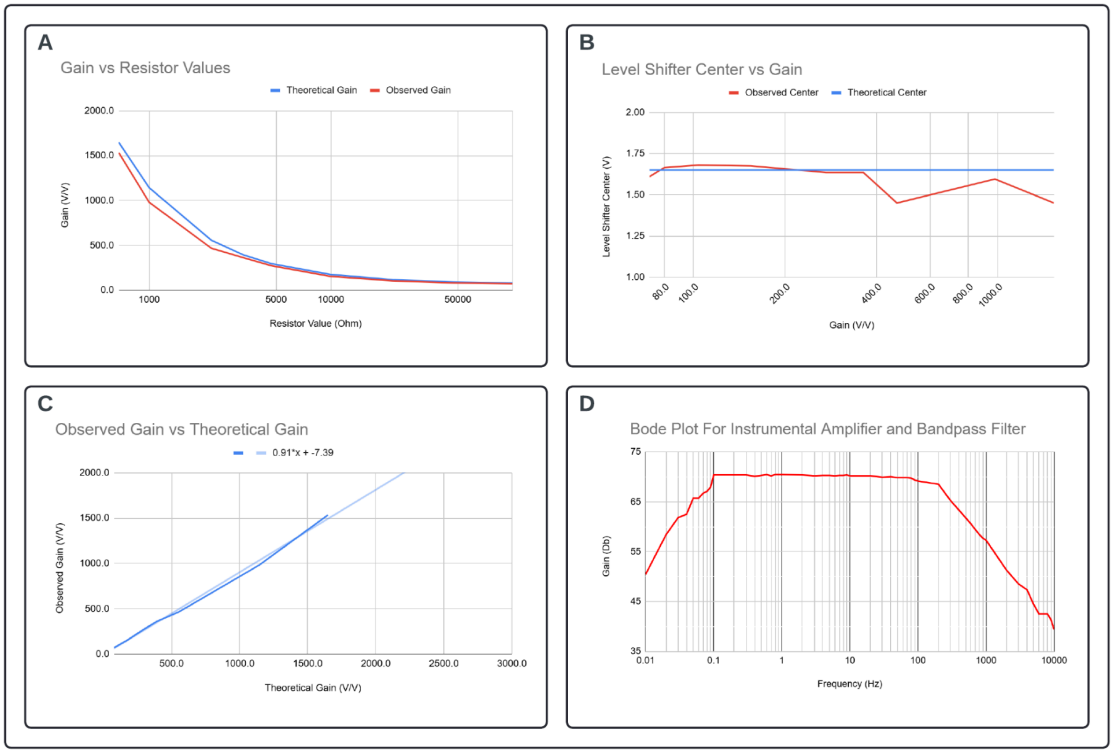

Figure 6: Manual Test Results for the Analog Front End. A. Gain vs Resistor values plot for the analog front end. B. Level shifter center vs gain plot. C. Observed vs theoretical gain plot with the linearly regressed projection. D. Bode plot of the frequency response for the populated third channel within the parallel series configuration. Note that the overall gain occurs at 50.47 dB, which is 333 V/V, and the passband frequency extends from .1Hz to 200 Hz.

Table I: Design Requirements Evaluation

Category	Design Requirement Value	Observed Value
Passband Range	0.1 to 150 Hz	0.1 to 200 Hz
Gain	2757/2857 V/V(parallel/serial)	2501/2592 (parallel/serial)
Level Shifter Center	1.65V	1.6±0.06V
Cost	$100	$61

c). Driven Right Leg

The driven right leg circuit was found to be non-functional, which is attributed to incorrectly extracting the common mode signal. The circuit is then revised to the following, where V_in1 and V_in2 are the two input signals and the common mode signal is extracted before being passed to the instrumentation amplifier (Figure 7).

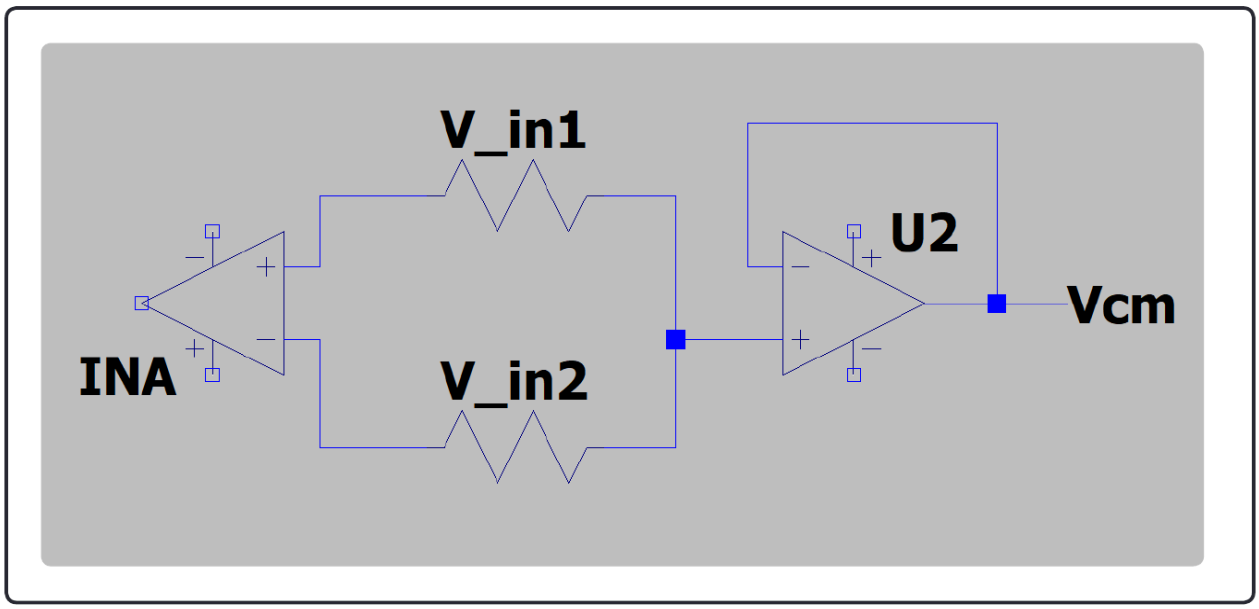

Figure 7: Proposed revision for extracting the common mode signal for the driven right leg circuit

B. Head Cap and Ear Clip

The testing for the ear clip was conducted to test the accuracy of the anatomical placements of the electrodes. For the first subject tested the mean absolute percent error and standard deviation was 5.80% ± 2.00. While for the second subject mean absolute percent error and standard deviation was 7.29% ± 13.2. This high standard deviation was likely due to the 10% and 90% landmarks being 41% and 11% off respectively, while all others were between -1.7% and 6.8%. This suggests that readings from the 10% and 90% nasion to inion landmarks may be less accurate for some individuals with this current design. The head cap did fit for both individuals with head circumferences around 55 cm, but did not for others who were closer to 60cm, suggesting that at least one other larger head cap of this current design will need to be created to meet the needs of the PDS. The raw testing data can be found in Appendix C.

The results from the ear clip comfort testing showed the effectiveness of the design. At the start, all participants rated the ear clip comfort as "Extremely Light" on the discomfort scale or an average of 7.25. At the end of the test, the team did see a 34.5% increase in the mean comfort level of the participants. An increase from 7.25 value to 9.75 was recorded (Figure 8). Throughout the test, some mechanical failures were encountered in the ear clip design itself. The clip started to show signs of permanent deformation. Another observation from the data was that the participants with attached earlobes had an increase in mean discomfort level of 1.5 for the initial and final surveys. This information shows that comfort is negligible for the current ear clip design. Moving forward, the team will focus on revising the ear clip design to create more durability. Further testing will be completed to test the durability of our new design.

Table II: Summary of the Discomfort Evaluation of the Ear Clips

Subject #	Comfort Level After 10 Seconds	Comfort Level After 10 Minutes
1	8	11
2	8	10
3	7	8
4	6	10

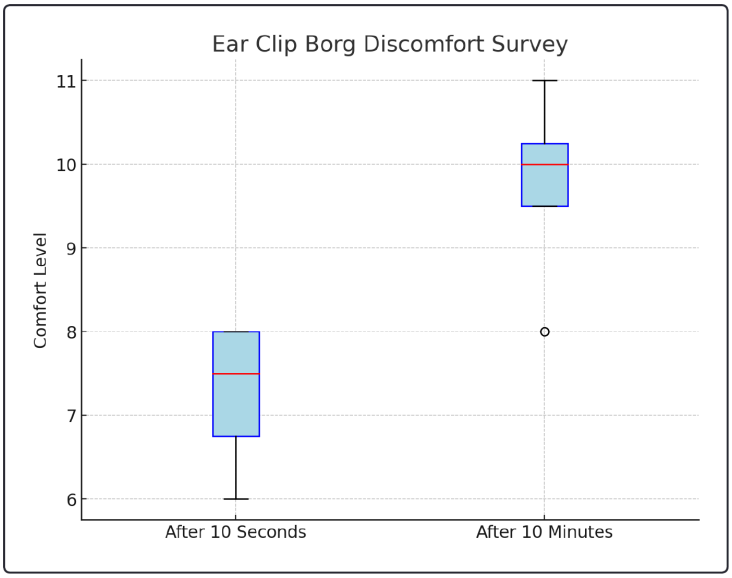

Figure 8: Box Plot Summary of the Borg Discomfort Survey for Two Participants

C. Embedded Systems

Upon initial testing, it was found that the interrupt timer using the add_repeating_timer_ms() function would not successfully be called at a frequency greater than about 800 Hz, it was found that the add_repeating_timer_us() function was needed instead. This was verified by having the interrupt function change the state high or low voltage of any GPIO pin and read the time between changes on an oscilloscope. Further testing will be performed to verify accuracy of code related to MUX, Digipot control. Upon verification of this section, the next focus will be on sending data over USB to an external PC where it will be shown on a live display and be recorded for later analysis as well as changing the resistance of R_{Rheo} in Equations 3-5.

IV. DISCUSSION

A. Driven Right Leg

Upon testing, it was discovered that the driven right leg did not produce the expected results. The resistor averaging network was deployed after the buffer stage of the instrumental amplifier, causing issues with obtaining an accurate common mode signal. To confirm this was the issue present, the averaging network was established in parallel with the instrumental amplifier on a breadboard. Testing was conducted by sending two signals of the same frequency but varying amplitudes through the circuit. The circuit was able to appropriately handle both signals, allowing the signal differential to pass through the rest of the circuit. This new topology of a parallel averaging network will be applied to version two of the PCB.

B. Gain Inaccuracies

The gain inaccuracies can be at least partially explained by resistor inaccuracies (5%). Assuming 5% deviation, a maximum deviation of +8.11 V/V to -8.96 V/V can be observed at the output of the instrumentation amplifier, +2.83 V/V to -2.56 V/V at the output of the bandpass filter, and +0.05 V/V to -0.05 V/V at the output of the level shifter. Taken together, a maximum reduction to an overall gain of 2015 V/V is possible due to resistors. Thus, our observed value can be well explained by resistor inaccuracies alone.

C. Hardware Revisions

Along with the driven right leg alterations, a few other updates will occur on version two. Testing will be conducted on the two different configurations to investigate how effective each circuit is at handling switching artifacts. A cost-benefit analysis will be conducted to select the appropriate topology that minimizes cost while aligning with the product design specifications. This configuration will be employed in all channels of version two. Additionally, components will transition to surface mount to decrease cost and increase accuracy. This includes all capacitors and resistors utilized throughout the circuit. All integrated circuits utilized on the PCB are surface mount and have functioned appropriately, and will thus be installed in version two.

D. Future Circuit Testing

To evaluate the accuracy and reliability of version two of this circuit, two major tests will be performed. The common mode rejection ratio will be determined by sending a signal with noise as well as a DC reference signal with noise. The common and differential gain will be calculated in order to successfully determine the rejection ratio, as seen in equation 6. The signal to noise ratio (SNR) will also be determined by feeding the circuit a signal and performing a FFT on the resulting output; equation 7 can then be utilized to calculate the SNR. Alongside these testing procedures, the circuit output will be observed on the GUI to ensure that no artifacts occur from switching between the 10 channels. The gain and passband of version two will also be calculated by the creation of a Bode plot for the entire circuit. The detailed testing protocols can be found in Appendix D-F.

$$CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}}) \tag{6}$$

$$SNR(dB) = 10 \times log_{10}(\frac{P_{signal}}{P_{noise}}) \tag{7}$$

E. Head Cap and Ear Clip

The head cap will undergo a complete design change in the second prototype. While conducting testing of the head cap, the 3D printed design was found to not fit certain head sizes. One of the design constraints is the head cap can fit all head sizes in order to conduct the EEG test. The necessity of a head cap is also a point of interest for the second revision. Placing the electrodes directly onto the head using a gel is something that will be tested against the use of a headcap. A fabric head cap that is elastic enough to fit a range of head sizes and shapes is another design idea for the future. Once the testing is complete to determine whether the head cap is needed or not, a test of the entire system will be conducted contingent on the completion of the previous system. The ear clip design must be altered in order to become more durable. During the previous testing, the ear clip encountered permanent deformation in the mechanism. Testing in the future will include durability testing as well as testing the electrode to ear interface using a pressure sensor.

V. CONCLUSION

A low cost EEG headcap could bring the availability of viral induced epilepsy testing to more of the 40 million users affected that may not otherwise be able to afford diagnostic testing. This design allows production of an open source 10 channel EEG headcap that can sample at 1 kHz with a 12 bit resolution for under $100. The team developed a TPU 3D-printed head cap, ear clips to house reference and driven right leg electrodes, and the analog front end on a PCB. The head cap shows a 5.8% to 7.3% mean absolute error in landmark alignment and could not fit on individuals with a head circumference above 60 cm. The ear clips were found to be comfortable among participants, with an initial average Borg score of 7.25 and a 10-minute score of 9.75. However, permanent inelastic deformation was observed during testing. The simulated frequency response of the analog front end (0.1 Hz to 163 Hz) matched its theoretical values and was confirmed by the manual Bode plot. The theoretical gain of the INA (200 V/V) matches the simulation results, but was observed to be only 33 V/V when manually tested.

The head cap shows good land mark alignment for individuals with head size of around 55 cm. However, larger and smaller sizes must be produced to accommodate different head shapes. Although the ear clip was comfortable, its mechanical properties needed to be improved by changing the material or its physical design. Lastly, a sinusoidal signal was able to be amplified by the analog front end with the correct frequency response; however, the gain of the overall circuits necessitates further investigation. Furthermore, the embedded system must be developed to elucidate the CMRR, PSRR, and SNR of the two circuit configurations to choose the one that is cost-effective and high-fidelity.

VI. ACKNOWLEDGEMENTS

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VIII. APPENDIX

Appendix A: Product Design Specifications

Function

Epilepsy is a common chronic neurological disease characterized by abiding recurrent seizures [1]. The most recent WHO report cites 50 million people affected worldwide, whose risk of premature death is up to three times that of the general population [2]. Electroencephalogram (EEG) is the most widely used detection and analysis procedure for epilepsy, which records cortical electrical activity. Identifying EEG patterns and seizure foci is critical for the diagnosis of specific epilepsy syndromes and, consequently, the selection of appropriate therapy [3]. However, 80% of epilepsy patients live in low- and middle-income countries, the majority of which do not have access to EEG systems or treatments [2]. Therefore, affordable EEG systems that can be rapidly and broadly deployed are in critical need.

Client requirements

- A single-channel sampling rate of at least 1 kHz.
- 12- to 16-bit analog-to-digital converter resolution.
- Periodic reading of electrode impedance to detect improper electrode contact.
- Total system cost at or below $100.
- 10-channel analog frontend.
- Driven by wall-plugged power supply.

Design requirements

Physical and Operational Characteristics

Performance requirements

The devices will be used for 20 to 40 minutes per patient per procedure [4]. The frequency of usage is dependent on the medical facility.

Safety

The device must be sanitized between uses, and the skin contact electrodes must be replaced. Since the device involves prolonged skin contact, irritation, discomfort, and allergic reactions are possible. The device consists of active electrical components and wires; thus, it must be carefully handled and not be tampered with while powered on. Furthermore, the device's temperature during operation must not exceed 40 ℃.

Accuracy and Reliability

The system should have a sampling rate of at least 1 kHz per client's requirement. The analog-to-digital converter (ADC) should encode with at least a 12-bit resolution to capture finer details of the EEG waveform. Low impedance, e.g., 5 k**Ω** electrodes, should be used to enhance signal clarity. To improve ease of use, the device should detect improperly connected electrodes. Additionally, signal filtering is required to reduce capacitive coupling effects from power lines and electromyogram interference.

Typically, the reliability of a diagnostic system is measured by its positive predictive value; however, the accuracy of epilepsy classification is critically dependent on monitoring duration and is unrealistic to calculate within the scope of this project [5].

Life in Service

The system must remain operational for 3-4 years with proper daily usage, ensuring durability and consistent performance. It should function effectively within a temperature range of 0-40°C without any drop-off in EEG signal amplitude, as higher temperatures are observed to negatively affect signal quality in existing EEG systems [6]. Additionally, the system must be easy to clean between uses, as it will be exposed to various cleaning products. The head cap should remain functional for 3-4 years with daily cleaning.

Shelf Life

The product should maintain its integrity and functionality in storage for at least ten years at room temperature. It must withstand transportation without any wear or damage and be designed to endure harsh conditions during transit. The product should tolerate storage temperatures ranging from -20°C to 100°C, as it may encounter extreme environments during transportation.

Operating Environment

The EEG cap must ensure consistent and secure contact between the electrodes and the scalp to accurately capture brain signals while maintaining user comfort over extended periods. The materials should be soft, lightweight, and non-invasive, providing a secure yet non-irritating fit. The EEG system should also function reliably in various temperatures typical of indoor and controlled outdoor environments, e.g., 0-40°C. The cap and circuit board should resist sweat, moisture, and mild physical impacts, ensuring long-term durability and accurate signal collection.

Ergonomics

The system should be accurate and fit users with a maximum horizontal head circumference between 50 to 64 cm, similar to other commercially available EEG electrode caps [7, 8]. The system should be effective for users of any hair volume and texture between bald and hair type 1 to 4d [9].

Figure 1. *Examples of hair types*

Size

The entire system should be portable and easy to carry. The cap and electrodes should be able to fit on most children and adults.

Weight

The system should weigh less than 1 lb and cause no neck strain while wearing.

Materials

There are no printed circuit board (PCB) materials restrictions as the device is not intended to operate in extreme environments. Operating temperatures, coefficient of thermal expansion, and electrical characteristics are non-critical factors. Dry electrodes are preferred, typically composed of conductive silicone or gold-plated electrodes, as requested by the client [10]. The head cap should resist cleaning solutions, e.g., ethyl or isopropyl alcohol and chlorine-releasing agents.

Aesthetics, Appearance, and Finish

The cap's design will ensure the patient feels comfortable in the environment. All wires should be as enclosed as the system allows. The circuit board will have a cover to shield the view from the patient. The appearance will be sleek and neutral to avoid any strong aversions. The appearance of the electrodes and the board will be professional in portraying the device's safety.

Production Characteristics

Quantity

One unit is needed for the scope of this project. This unit should be created to be reproducible on a large scale.

Target Product Cost

For one unit, the entire system costs at or below $100.

Miscellaneous

Standards and Specifications

The Code of Federal Regulations Title 21, Volume 8 Chapter 1 Part 882: Neurological Devices provides specific standards concerning electroencephalograms (EEGs) and other commercially distributed neurological devices intended for humans. Sec. 882.1400 states that EEGs are used to measure and record the brain's electrical activity and are classified as a class II medical device [11]. This means they have to follow general regulatory control and special controls, including performance standards, special labeling requirements, and post-market surveillance [12]. They must also go through the 510(k), a premarket submission process that proves the device is similar to one currently operating and showcases that it is safe [13]. To be considered within this classification, the EEG can have recording hardware, monitor, and basic software; however, this does not include electrodes, a complex software analysis system (to either auto-detect or analyze events), or a system with more than 16 electrodes. Additionally, this device is not allowed to be used in sleep studies. EEG electrode/lead tester is a device used to test the impedance of electrodes. It is classified as a Class I device, along with an EEG signal spectrum analyzer and an EEG test signal generator. Cutaneous electrodes are applied directly to the skin to record or apply electrical stimulation and are classified as a Class II medical device.

In addition to FDA standards, IEEE recommended practice for EEG Neurofeedback Systems details practices that should be abided by [14]. The system must adhere to the IEC 60601-1 Safety and Essential Performance standard to follow safety procedures. The EEG should be sold as a medical device, where the user is trained to operate the equipment properly. System software shall be available to allow all parts of the system to be analyzed as needed. This includes electrodes, which should have an expected lifetime, performance, polarization rate, and long-term stability. Cleaning techniques, application, and impedance checking should accompany these electrodes. Several different specifications should be included for the primary component, as listed in Table 1.

Along with these documents, several ISO and IEC standards are applicable. IEC standard 80601-2-26:2019 details the particular requirements for EEGs' basic safety and performance [15]. ISO standard 22077-5:2021 specifies the format of waveforms created during EEG to support one recording session [16].

***Table II**: Specifications that must be listed, as stated by IEEE Recommended Practice for EEG [14]*

Amplifier Specifications	**Frequency specifications**	**Analog to Digital Conversion**
Input impedance	Magnitude response	Number of bits, number of channels, and type input/output channel
DC/AC coupling (time constant if ac coupled)	Phase response	Sampling rate
Noise/sensitivity (RMS and/or peak-peak voltage, given bandwidth or application, noise spectrum)	Corner frequency / frequencies	Anti-aliasing filter specification
Signal input range	Decay and rolloff	Resolution, quantization error, and/or least-sig bit size (eg performance over temperature, hysteresis, etc.)
Signal output range	Decibel (dB) attenuation in stopband	ADC technique
Ground type (active/not) or direct reference line noise		Channel-to-channel isolation and digital channel
CMRR		
Gain		
Bandwidth		
Supply voltage/current consumption		
Impedance checking specifications (stimulus, measurement time/duration, absolute accuracy, relative accuracy)		
Amplification		

Customer

The device is tailored for medical clinics in underdeveloped areas; thus, its cost and durability are prioritized. Borth criteria are detailed in this document above. Additionally, the device should be intuitive to use and include detailed instructions in various languages.

Patient-related concerns

Four main patient-related concerns will be addressed:

- **Patient Comfort & Skin Irritation**: Long-term EEG monitoring may cause discomfort or skin irritation, especially due to the electrodes' contact with the scalp. Proper cap design, skin preparation, and using hypoallergenic materials are essential to reduce discomfort and prevent rashes or sores.
- **Movement Restrictions**: Patients must remain relatively still during EEG recording to avoid artifacts from muscle movements. This can be challenging, especially for pediatric or uncooperative patients, leading to inaccurate readings.

- **Infection Risk & Hygiene**: Reusing EEG caps and electrodes poses a risk of infection if they are not properly sanitized between uses. Ensuring strict hygiene protocols and using disposable components when necessary can mitigate this risk.
- **Psychological Stress or Anxiety** Some patients, particularly children or those with certain neurological conditions, may experience anxiety or discomfort during the EEG process due to unfamiliar equipment or the need to remain still for extended periods. Clear communication and a calming environment can help alleviate these concerns.

Competition

Most EEG systems are intended for medical use and are inaccessible to consumers and medical facilities in underdeveloped countries. Although consumer EEG systems with relatively low costs exist, none of the multi-channel systems cost close to the $100 threshold (Table III). Commercialized products like Neurosky, Muse, and Emotiv often feature non-essential Bluetooth functionalities and auxiliary sensors that contribute to their cost. Their channel count and sampling rate also fall short of the client's requirements. Open EEG's modular EEG system offers the most competitive pricing for its performance. However, its ATmega8 employs a 10-bit ADC with six channels that fail to meet the performance requirements.

***Table III**: Summary of Existing Consumer EEG Devices*

Product	Channel Count	Sampling Rate (Hz)	Bit Depth	Wireless	Cost (USD)
Neurosky MindWave	1	512	12	Yes	130
Muse2	4	256	12	Yes	300
Emotiv MN8	2	128	14	Yes	400
Emotiv Insight	5	128	16	Yes	500
Emotiv EPOC X	14	256	14-16	Yes	1000
Emotiv Flex Saline	32	256	16	Yes	2000
Open BCI Complete Kit	16	125	24	No	2500
Open EEG	2-6	Up to 15.4k	10	No	200-400

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Appendix B

Table IV: Head Cap Design Matrix

	Store Bought		3D Print		No Head Cap		DIY		
									
	Points out of 5	**Weighted Score**							**Weight**
Cost	0	0	4	80	5	100	4	80	**20**
Safety	5	75	4	60	3	45	3	45	**15**
Accuracy	5	70	4	56	1	14	2	28	**14**
Repeatability	4	56	5	70	1	14	2	28	**14**
Ease of Use	5	65	4	52	2	26	2	26	**13**
Durability	5	60	3	36	4	48	2	24	**12**
Comfort	5	35	4	28	4	28	3	21	**7**
Ease of fabrication	5	25	2	10	5	25	3	15	**5**
Total		**386**		**392**		**300**		**267**	**100**

Cost:

The expected cost to produce one electrode cap. Store Bought is by far the most expensive, with most models being well over $100, No Head Cap requires no additional material so is therefore the cheapest. DIY and 3D Print have the potential to be inexpensive depending on material choice, but do have some cost associated with them.

Safety:

All electrode caps should be safe for use and provide stable electrode connection, while none of these designs provide major risk, Store Bought was most safe since it provides the most protection between the electrodes and head while other designs may be at higher risk for electrodes to come loose.

Accuracy:

The electrode cap design must keep each electrode accurately at the associated biological marker. Store bought was ranked the most accurate since with more material covering the head, strain to cause electrode drift to incorrect locations is minimized by more material. No head cap is the least accurate since it requires

the Doctor to place electrodes manually before each test.

Repeatability:

The design must be able to be constructed and run repeatedly with no dip in performance of the product. The environment, patient, and the person running the test are all factors that could change. Despite these changes, the results should remain consistently accurate. The 3D printed design was ranked the highest because the team would have control over the production of each component unlike the store bought. The no head cap and DIY both ranked lower as these have a much higher chance of human error leading to less accurate results over multiple trials.

Ease of Use:

Ease of use refers to the difficulty for the tester to run the test on the patient. This product needs to be fairly easy to use so that a trained operator can consistently give the test and the patient has no issues during the test. The store bought design ranked highest because the commercial products are tailored to the interest of the consumer, giving it a good chance to be easy to use. The DIY and no head cap ranked lowest as these would require a lot more training on how to create/execute the test.

Durability:

This design must be durable in order to withstand travel, repeated use, and movement as the patient adjusts the product in order to fit the cap to their head. The store bought design was ranked the highest as since these are commercially available, the quality of the product will most likely be higher than our other design ideas. The no head cap scored higher on this metric as there is not much that could be damaged to the product itself. While the DIY and 3D printed designs have a higher chance of human error as well as a design tailored to performance and not durability.

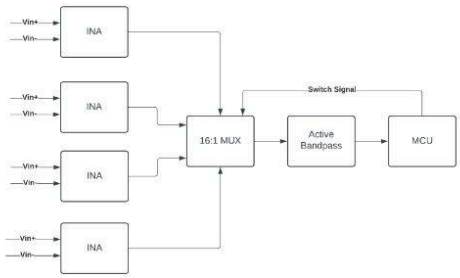
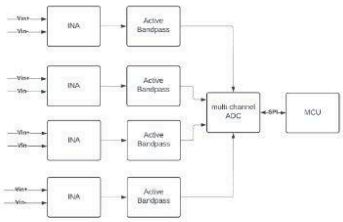
Comfort:

The design must be comfortable enough for the patient to get through the test without any difficulties but the team decided this was not of top priority due to the importance of other factors. The store bought design ranked the highest amongst this metric as since those are typically more expensive the company creating the design has put more effort into the comfort of the product than our other designs. The DIY ranked the lowest as this design would be very simplistic and tailored towards accomplishing the task of running the test accurately without a focus on comfort.

Ease of fabrication:

Ease of fabrication was not weighted as highly as other factors due to most of these products being easy to assemble. The 3D printed design ranks the lowest as this would be the most difficult to fabricate due to the size and structure of the cap itself. The store bought would be easily fabricated as there would be no assembly, the cap would arrive fabricated.

Table V: Analog Front End Design Matrix

			
	Single-channel ADC + MUX	**Multi-channel ADC**	**Weights**
Cost	26	16	26
Accuracy	16	21	26
Ease of fabrication	20	15	25
Firmware Complexity	5	3	5
Components Availability	14	10	17
Sum	**81**	**65**	100

Cost:

Cost is defined as the listed price of the component on Digikey. The cost for creating the single-channel ADC + MUX costs less to produce, as the multi-channel ADC costs significantly more than the single channel ADC.

Accuracy:

Accuracy is defined as the amount of noise contributed by the individual component. There are less components in the multi-channel ADC, so there is less probability of noise being created. However, neither circuit was given a 5, as the components will generate some amount of noise. This will particularly be true due to the low cost objective; more noise will likely enter the signal acquisition as a result of using cheaper components.

Ease of fabrication:

Ease of fabrication is defined as the amount of time and effort that it takes for the team to fully assemble the system, e.g., soldering, PCB designs. The multi-channel ADC has less individual components, so it will be easier to fabricate.

Firmware Complexity:

Firmware complexity is defined as the associated coding and wiring complexity. The multi-channel ADC received a higher score because of the ease of coding. Creating the code to alternate through each electrode channel is more difficult that reading all of the separate signals at once.

Component Availability:

Components availability is defined as the number of equivalent components available on Digikey. Equivalency refers to the ability of the component being swapped without changes to other components. There are more equivalent swaps for the creation of the single channel circuit, so it was given a higher rating.

Appendix C Head Cap Testing Data

Table VI: Raw Data from Head Cap Landmark Alignment

Subject 1								Subject 2							
% distance from nasion landmark to inion	Measured Distance (cm)	Expected Distance (cm)	Difference	Percent Error	Mean absolute Percent Error	Median absolute percent error	Standard Deviation	% distance from nasion landmark to inion	Measured Distance (cm)	Expected Distance (cm)	Difference	Percent Error	Mean absolute Percent Error	Median absolute percent error	Standard Deviation
10%	3.5	3.8	-0.3	-7.89	5.80	5.26	2.00	10%	5.5	3.9	1.6	41.03	7.29	1.71	13.2
20%	7	7.6	-0.6	-7.89				20%	8	7.8	0.2	2.56			
30%	11	11.4	-0.4	-3.51				30%	12.5	11.7	0.8	6.84			
40%	14.5	15.2	-0.7	-4.61				40%	15.5	15.6	-0.1	-0.64			
50%	18	19	-1	-5.26				50%	19.5	19.5	0	0.00			
60%	22	22.8	-0.8	-3.51				60%	23	23.4	-0.4	-1.71			
70%	29	26.6	2.4	9.02				70%	27	27.3	-0.3	-1.10			
80%	32	30.4	1.6	5.26				80%	31	31.2	-0.2	-0.64			
90%	36	34.2	1.8	5.26				90%	39	35.1	3.9	11.11			

Appendix D: PSRR Testing Protocol

PSRR = 20 log (Δvin/Δvout)

Materials

1. AC+DC network summing device
2. Oscilloscope (ideally one that can automate frequency sweep)

Protocol

1. Connect 5V DC to the summing device and an AC 60 Hz source with 100mV PtP
2. Connect the recording electrode and reference to 1V DC
3. Observe the PtP ripple amplitude at Vout
4. calculate PSRR

Appendix E: CMRR Testing Protocol

Stage 1 - Testing without Mux

1. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.
2. Hook up the input of the first instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes of the first instrumental amplifier.
3. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.
4. Apply a 20Hz 100 μV sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 μV sine wave to the wave generator that is attached to both the input and reference input.
5. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.
6. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.
7. Perform calculations using the equation $CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}})$, where the $G_{differential}$ is the value of the output at 20Hz, and G_{common} is the value of the output at 60Hz. Both the $G_{differential}$ and G_{common} should be expressed in voltage.
8. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.
9. Repeat this protocol with 5Hz, 10Hz, 15Hz, 25Hz, and 30Hz all replacing the 20 Hz signal, keeping the signal amplitude at 100 μV.

Stage 2 - Testing with Mux

10. Place the circuit board on circuit, connecting all necessary components that are not permanently attached. Inspect the circuit board to ensure that all connections are solid and all components are placed correctly.
11. Hook up the input of the instrumental amplifier to a wave generator, and hook up a second wave generator to both the input and reference nodes. All of the inputs for the instrumental amplifier should receive the same signal, as should all of the reference nodes.
12. Set up three oscilloscope probes, one to measure the input at the instrumental amp, one to measure the input at the reference probe, and one to measure the output of the circuit.

13. Apply a 20Hz 100 μV sine wave to the input of the instrumental amplifier. Apply a 60 Hz, 10 μV sine wave to the wave generator that is attached to both the input and reference input.

14. Collect the data from running the test for 10 seconds. Ensure that the data fills the screen without cutting any off.

15. Inspect the data and note anything of significance that could account from the addition of the mux. This can include spikes or lapses in data.

16. Perform a FFT on the collected data. This can be done by selecting the FFT option on the bottom of the oscilloscope. Note the values that are displayed for both 20 Hz and 60Hz.

17. Perform calculations using the equation $CMRR(dB) = 20 \times log_{10}(\frac{G_{differential}}{G_{common}})$, where the $G_{differential}$ is the value of the output at 20Hz, and G_{common} is the value of the output at 60Hz. Both the $G_{differential}$ and G_{common} should be expressed in voltage.

18. Perform this experiment 5 separate times by allowing the circuit to run for 10 seconds, analyzing that data, then allowing the circuit to run to collect the next sample.

19. Repeat this protocol with 5Hz and then 30Hz replacing the 20 Hz signal, keeping the signal amplitude at 100 μV.

Appendix F: Commercial EEG Comparison

Material

- Tucker-Davies Technology recording cart
- EEG testing board
- 5-6 gold cup electrodes
- electrode gel/cream
- abrasive gel/paper towel
- tape measure
- marker
- gauze

TDT setup

- The recording and reference electrodes are attached to the TDT amplifier
- recording software is opened and ready to record

PCB setup

- The EEG PCB board should be connected to a computer via a micro USB cable.
- The recording, reference, and DRL electrodes are attached to the board.
- Appropriate recording software/terminal is opened and ready to record

Procedure

1. Identify attachment location according to the 10/20 standard.
    1. Use a tape measure to drape across the head to coincide with the sagittal plane.
    2. Make sure the tape measure begins at the nasion and ends at the inion.
    3. Mark the skin at 10% of the length from the nasion (Fp1).
2. Clean the skin at the location and use abrasive gel or paper towel to reduce impedance.
3. Apply electrode gel to the gauze.
4. Apply adequate electrode gel to the cup electrode and place the stem of the electrode on the gelled gauze

5. Press gently on the skin
    1. repeat for the two recording electrodes and others
6. begin recording
7. end recording after 5 mins
8. align recordings
9. adjust for sampling frequency if there is any difference
10. calculate dB error
    1. 20log(ground truth/PCB)
11. calculate variance and mean

Appendix G

Table VII: Electronics Cost

Component	Manufacturer	Manufacturer Part#	Cost Each	QTY	Total
Instrumentation Amplifier	Texas Instrument	INA827AIDGKR	1.906	10	19.06
Multiplexer	Texas Instrument	CD74HC4067M96	0.66	1	0.66
Digital Rheostat	Microchip Technology	MCP40D17T-104E/LT	0.68	1	0.68
Microcontroller	Rasberry Pi	RP2040	4	1	4
Operational Amplifier	Texas Instrument	TLV9004IDR	0.66	1	0.66
Operational Amplifier	Texas Instrument	TL072CDR	0.3	1	0.3
Male Header	Samtec	HTSW-108-07-G-D	0.9	1	0.9
.1uF capacitor	KEMET	C320C104K5R5TA	0.23	55	12.65
10uF capacitor	KEMET	C324C106K3R5TA	0.94	9	8.46
100uF cappacitor	Würth Elektronik	860010372006	0.1	1	0.1
220pF capacitor	Nichion	URZ1HR22MDD1TD	0.3	6	1.8
DC-DC convertor	Microchip Technology	TC962EPA	4.09	1	4.09
10K Resistor	Stackpole Electronics	CF14JT10K0	0.1	18	1.8
20K Resistor	Stackpole Electronics	CF18JT20K1	0.1	16	1.6
390K Resistor	Stackpole Electronics	CF14JT390K	0.1	4	0.4
160K Resistor	Stackpole Electronics	CF14JT160K	0.1	6	0.6
470 Resistor	Stackpole Electronics	CF14JT470R	0.1	6	0.6
1K Resistor	Stackpole Electronics	RNF14FTD1K00	0.1	2	0.2
360 Resistor	Stackpole Electronics	CF12JT360R	0.1	8	0.8
180 Resistor	Stackpole Electronics	CF14JT180R	0.1	4	0.4
4.3M Resistor	Stackpole Electronics	CF14JT4M30	0.1	6	0.6
				Total	53.36

Appendix H

Table I: Manufacturing Parameters of the PCB

Parameter	Value
Size (mm)	135.8×114.3
Thickness (mm)	1.6
Minimum Hole Size (mm)	0.3
Material	FR-4 TG 150-160
Layers	2
Via Process	Tenting Vias
Finished Copper (oz)	1
Surface Finish	Hot Air Solder Leveling with Lead
Minimum Track Width (mil)	6
Minimum Track Spacing (mil)	6

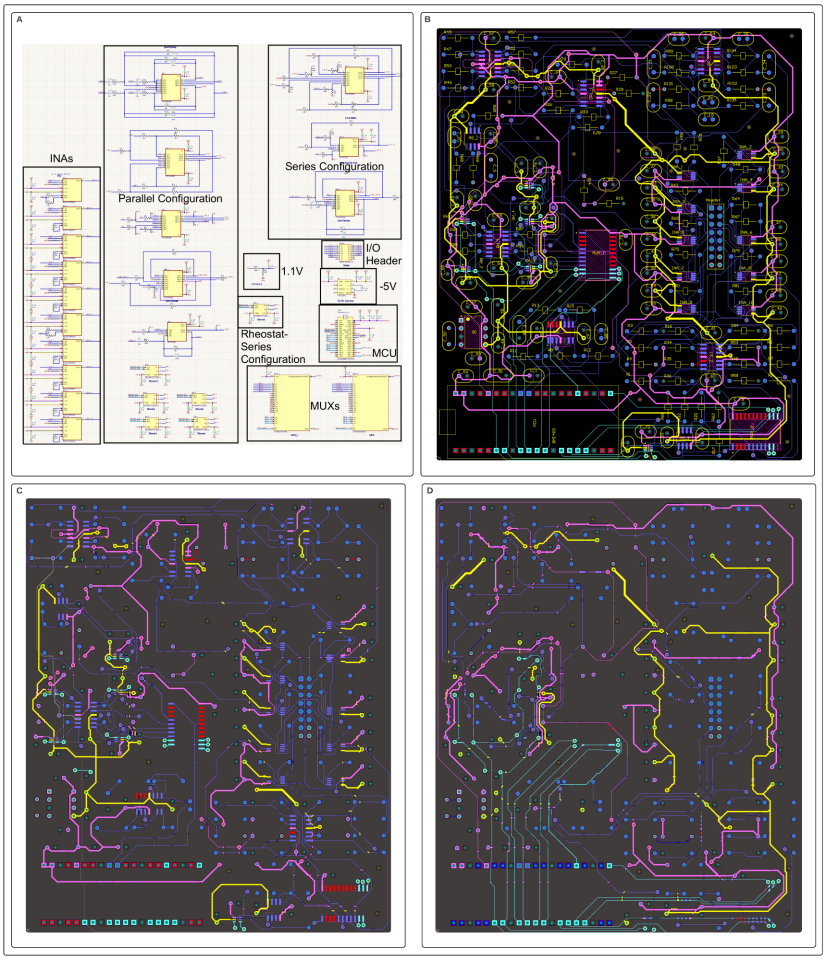


Figure 7: Final Design of the PCB. A. Final schematic diagram of the PCB. B. Front side of the PCB without polygon fills. VCC and VEE are colored pink and yellow, respectively. Analog signals are colored purple, and digital signals are colored cyan. C.

Front side of the PCB with polygon fills and hidden silkscreen. The ground signal is colored grey. D. Backside of the PCB with polygon fills and hidden silkscreen.